Century Data Systems—MODEL 114 DISK DRIVE TECHNICAL MANUAL

MODEL 114 DISK DRIVE

TECHNICAL MANUAL

RECORD OF REVISIONS	
REVISION	**NOTES**
J 10-22-73	Releases J Revision, incorporating new format and style.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

INTRODUCTION

GENERAL

This manual contains information pertaining to the installation, operation, theory of operation, and maintenance of the Model 114 Disk Drive. A Model 114 (Figure 1-1) has a single disk drive per cabinet.

SCOPE

This manual is intended as a maintenance document as well as a training document for customer engineers. The manual is divided into two volumes:

Volume I:

- Section 1 —General Information
- Section 2 — Installation, Checkout, and Operating Procedures
- Section 3 — Theory of Operation
- Section 4 — Preventive Maintenance
- Section 5 — Checks, Adjustments and Replacements

Volume II:

- Card Schematics and Logic Diagrams

RELATED DOCUMENTATION

Related documentation is not listed as this manual is all inclusive except for the physical planning manual (PPCDS) and parts catalog (PC114).

INTRODUCTION

The Model 114 Disk Drive is a high-speed, random-access memory device designed for mass data storage in data processing systems. A maximum of nine drives (eight on-line and one off-line) can be connected to a single controller. The controller provides the data and control interface between the drives and central processing unit I/O interface.

The disk drive can be divided into the following basic functional areas:

- Input/Output Interface
- Read/Write System
- Positioning System
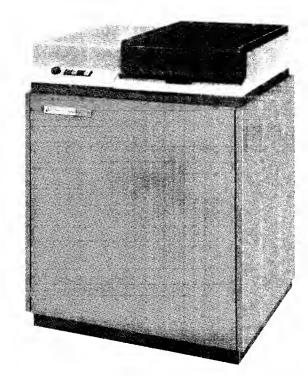
Figure 1-1. Model 114 Disk Drive

Figure 1-2 shows and describes the functional areas. The following paragraphs provide a general description of the disk drive and highlight the significant electromechanical areas.

INPUT INTERFACE

The controller provides the following input interface to the drive:

- Address select lines
- Bus and tag lines
- Write data line

There are nine address select lines connected in series-parallel to each drive. When the controller selects a drive, one of the address lines is activated. An address

FROM CONTROLLER   WRITE OATA   **READ/WRITE SYSTEM**   REAO DATA   TO CONTROLLER

READ/WRITE SYSTEM
- READ/WRITE ELECTRONICS
- ADDRESS REGISTER
- READ/WRITE HEADS
- DISK PACK

STATUS

OUTPUT INTERFACE
- LATCHES
- FLIP-FLOPS
- MONITOR LOGIC
- DRIVERS

INPUT INTERFACE
- RECEIVERS
- DECODE LOGIC

WRITE — CONVERTS DATA FROM CONTROLLER TO MAGNETIC RECOROINGS

READ — CONVERTS MAGNETIC RECOROING TO DATA FOR CONTROLLER

FROM CONTROLLER

COMMANOS AND AOORESSES

DECOOES BUS AND TAG LINES FROM CONTROLLER

PROVIDES STATUS OF ALL SIGNIFICANT EVENTS TO CONTROLLER

TO CONTROLLER

POSITIONING SYSTEM
- ADDRESS REGISTER
- LINEAR MOTOR
- SERVO LOGIC
- SERVO ELECTRONICS

STATUS

POSITIONS REAO/WRITE HEADS AT LOCATION SPECIFIED BY CONTROLLER

Figure 1-2. Model 114 Disk Drive, General Block Diagram

comparison scheme then enables the input and output interface logic if the address line agrees with the disk drive address.

There are eight bus lines and four tag lines which are used to present information to the drive. The four tag lines define the information on the bus lines as either addresses or control commands.

A bidirectional cable is used to route write data to the drive and read data to the controller. Write data is not controlled by the interface logic. However, the write enable lines are decoded from the bus and tag decode and are therefore controlled.

OUTPUT INTERFACE

Upon selection by the controller, the output interface is enabled and the following information is presented to the controller:

- A logic level indicating logical connection to the controller
- Present position of the read/write heads
- Positioning system status
- Error condition status

READ/WRITE SYSTEM

The read/write system includes the disk pack and the read/write heads.

Disk Pack

The disk drive uses a removable, eleven-high disk pack as the storage medium. Information is recorded on or read from the disk pack by twenty read/write heads, one for each recording surface. The read/write heads are mounted in a vertical stack on a single carriage assembly, and therefore move together over their respective disk surfaces. A linear motor attached to the head carriage moves the head carriage to position the read/write heads within the disk pack.

The disk pack contains eleven equally spaced aluminum disks stacked on a central hub. Each disk surface is coated with magnetic-oxide, providing 20 useable recording surfaces, with a protective disk at the top and bottom.

The bottom disk (sector/index disk) is slightly larger, in diameter, than all other disks. In the standard drive, the sector/index disk contains a single notch (index) which is used to detect disk pack rotational speed.

In Original Equipment Manufacture (OEM) applications, the sector/index disk may contain several equally spaced notches (usually 20) in addition to the index notch. The sector notches are used to divide each disk surface into equal areas for recording format purposes.

Data is recorded by magnetizing digital bit patterns in concentric circles (cylinders) on the recording surfaces. As shown in Figure 1-3, each surface contains 203 cylinders spaced at 0.010-inch intervals. The cylinders are numbered 000 through 202, beginning with the cylinder nearest the outer edge of the disk. Within a disk pack, all cylinders having the same number lie in the same vertical plane.
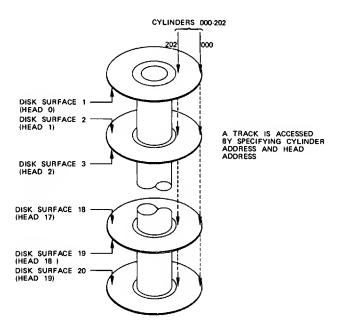
Figure 1-3. Cylinder Concept

The read/write heads are mounted so that head 00 moves over recording surface 00, head 01 moves over surface 01, etc. Each head is aligned so that they all lie in the same vertical plane. Therefore, when the head carriage is moved to one of the cylinder positions, each read/write head is positioned over a corresponding track on its recording surface. For example, when the head carriage is moved to cylinder 073, head 00 is positioned over track 073 on surface 00, head 01 is positioned over track 073 on surface 01, etc.

To select a particular track for recording or retrieval of data, the following is performed:

● The head carriage is moved to the cylinder containing the track to be accessed
● The read/write head that serves the desired track is then selected

A complete track address therefore consists of two parts, a cylinder address and a read/write head address.

Read/Write Head Operation

A read/write head is essentially an electromagnet that can concentrate a high magnetizing force over a very small area of the adjacent recording surface. When writing data, the flux field is alternated to magnetize the disk with the desired bit pattern. Each read/write head also contains a straddle-erase electromagnet; the function of which is to erase the edges of the data track just written. The width of each track is narrowed to approximately 0.005-inch by this erase method to minimize interference and crosstalk between adjacent tracks.

When reading data, the read/write electromagnet operates as a sensor. A flux reversal in the recorded track induces a voltage across the electromagnet coils. This voltage is amplified and conditioned to recover the recorded data.

Flying Head Principle

Figure 1-4 shows construction of a typical read/write head. Note that the read/write straddle erase coils are mounted on a single large pad. The head pad rides (flies) on a thin layer of air that adheres to the disk surface as it rotates. A very high air pressure is formed under the head pad. This pressure tries to lift the pad away from the disk surface. The head mounting arm incorporates spring tension which counteracts the air pressure and holds the head pad in the air stream. The read/write head arm tension is carefully controlled so that all read/write heads fly at approximately the same height (about 125-microinches from the disk surface). Since the read/write head does not actually contact the disk surface, head wear due to friction is essentially eliminated.
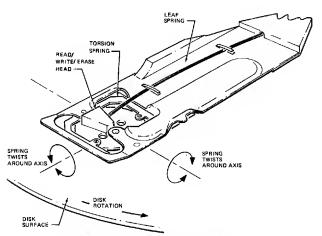
Figure 1-4. Read/Write Head Details

POSITIONING SYSTEM

The read/write heads are moved into place by a linear motor, which consists of a stationary permanent magnet surrounding a moveable, servo-driven voice coil armature (Figure 1-5).
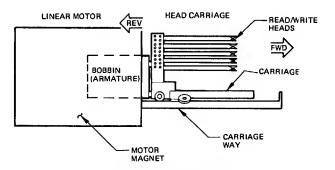
Figure 1-5. Access Mechanism

Power for the linear motor is provided by a direct current which flows in the armature. The magnetic field built up around the armature by this current reacts with the permanent magnet field and the reaction either forces the armature out away from the permanent magnet or pulls it into the field. Direction of travel depends on the polarity of current; speed depends on the amplitude of the current.

Fastened to the armature is a tower which holds the read/write heads. The tower is mounted on a carriage that moves freely along tracks on ball-bearing rollers. Movement of the armature in and out of the permanent magnet moves the carriage forward and backward. This linear travel positions the read/write heads over their respective disk surfaces or pulls them out and away from the disk pack. Moving the read/write heads into the pack is called loading the heads; retracting them from the pack is called unloading the heads.

Cylinder Transducer

Cylinder detection is accomplished by using a variable-reluctance transducer that senses the passing of teeth on a rack mounted on the head carriage (Figure 1-6). Each tooth on the rack corresponds to a specific cylinder. Thus, the number of teeth detected directly indicates the number of cylinder positions crossed while moving the read/write heads to a new cylinder position.
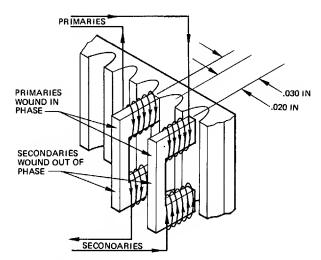
Figure 1-6. Cylinder Transducer/Rack Relationship

SECTOR/INDEX TRANSDUCER

As the disk pack rotates, an index notch in the bottom protective disk passes through a variable reluctance transducer field (Figure 1-7). The transducer generates a pulse each time a notch is sensed. In the OEM application there may be several equally spaced notches (sector notches) in addition to the index notch. For OEM applications, logic circuits monitor the transducer output for two adjacent pulses, thereby detecting passage of the index notch. The resultant index pulses are used to define the start of each recorded track.

In addition, the sector/index transducer is used to monitor the disk pack rotational speed. This is accomplished by checking the time between index pulses.
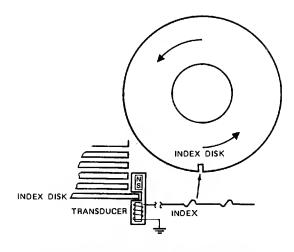
Figure 1-7. Sector/Index Disk and Transducer Details

DISK PACK SPINDLE AND DRIVE MOTOR

The disk pack spindle is mounted on the upper deck plate surface and is driven by a 208 vac drive motor. The motor and spindle are coupled by a pulley and belt system designed to provide a disk pack rotational speed of 2400 rpm. The motor provides high starting torque and as it accelerates, an internal centrifugal switch changes the motor windings to provide approximately 3450 revolutions per minute. The high speed is reduced to 2400 rpm by different diameter pulleys on the motor and spindle. The disk pack normally reaches full speed in approximately ten seconds.

The loading and removal of disk packs is facilitated by the spindle lock which prevents spindle rotation when the pack access door is open. A mechanical linkage, activated by opening the door, pushes the spindle locking arm into a notch in the spindle collar under the deck plate and holds the spindle in place so the pack mounting shaft can be tightened or loosened.

When a disk pack is installed, the spindle shaft is drawn up and the pack switch interlock is closed. The switch is located under the deck plate at the end of the spindle shaft. The interlock is used to detect the presence of the disk pack and to prevent drive motor operation when a disk pack is not installed.

AIR SYSTEM

Air for cooling and pack chamber pressurization is supplied by a blower located in the bottom of the cabinet. Intake air passes through a prefilter in the bottom of the cabinet and is filtered again at the input to the blower assembly. The air is then routed through an air shroud filter (absolute filter) to remove any remaining dust particles. The filtered air flows into the disk pack area at the spindle opening. The pack shroud forms a positive pressure chamber when sealed by the closed door. The positive pressure environment helps prevent head or disk damage by preventing small foreign particles from entering the pack area.

Air is also forced up into the disk pack hub through a filter in the bottom of the pack. Outlets in the hub provide clean air to maintain an air bearing over the recording disk surfaces.

PHYSICAL AND ELECTRICAL CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Height	40.25 inches
Width	30.00 inches
Depth	24.00 inches
Weight	350 pounds

POWER REQUIREMENTS

Input Voltage	208 or 230 vac ±10%, 3-phase or single phase
Line Frequency	60 Hz ±1% (50Hz ±1% optional)
Starting Current	15 amps for 5 seconds
Operating Current	3.5 amps rms

OPERATING ENVIRONMENT

Temperature	60°F to 90°F (maximum gradient of 20°F per hour
Relative Humidity	10% to 80% (no condensation)
Heat Dissipation	1570 btu per hour
Air Flow	200 cfm minimum

SPECIFICATIONS

Disk Pack	IBM 2316 or equivalent
Disk Pack Capacity Per Disk Pack	(Format Dependent) 233,408 million bits/29,176 million 8-bit bytes
Per Cylinder	1,152 million bits/144,000 thousand 8-bit bytes
Per Track	57,600 thousand bits/7,200 thousand 8-bit bytes
Recording Format	Fixed or variable length, IBM compatible
Recording Method	Double frequency, bit serial
Data Transfer Rate	2.5 million bits/312 thousand 8-bit bytes/second
Data Bit Cell Time	400 nanoseconds
Rotational Speed	2400 ±2% rpm/25 ±0.5 milliseconds/revolution
Rotational Latency Average Maximum	 12.5 milliseconds 25.0 milliseconds
Recording Cylinders	203 cylinder; 000 to 199 plus 3 spares
Cylinder Spacing	0.010-inch (nominal)
Recording Surfaces	20, one per read/write head
Read/Write Heads Recorded Track Width Straddle-Erase Width	20, Straddle-erase type 0.007-inch (nominal) 0.005-inch (nominal)
Head Positioning Time Maximum Average Maximum	 12 milliseconds/ cylinder-to-cylinder seek 35 milliseconds/average seek 65 milliseconds/203 cylinder seek
Start/Stop Time Start Stop	 22 seconds (drive ready) 10 seconds (dynamic braking)
Controllers	IBM 2314, CDS 1014, or equivalent

SECTION 2

INSTALLATION

GENERAL

This section provides procedures to ensure the operational integrity of the drive prior to on-line operation. If any adjustment or corrective action is required, enter the corrective action required on the Installation Completion Form.

INSTALLATION CHECK LIST

The installation check list (Table 2-1) is designed for trained service personnel to use as a guide in performing installation checks necessary for proper operation. If more detailed installation information is desired, refer to the appropriate paragraph in this section.
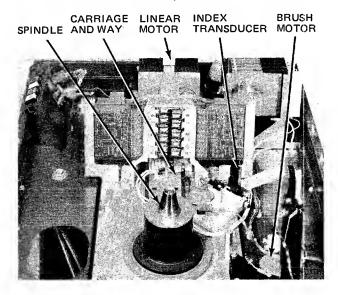
Table 2-1. Installation Check List

Visual Inspection	Input Ac Power
☐ a. Remove all packing material.	☐ a. If input ac power is between 190 vac and 218 vac, connect input power lead to 208 vac input terminal at rear of power supply chassis.
☐ b. Check for shipping damage.	
☐ c. Check for electrical short circuits.	☐ b. If input ac power is between 219 vac and 253 vac, connect input power lead to 230 vac input terminal at rear of power supply chassis.
☐ d. Check for loose or shorted wire connections.	
☐ e. Check and clean disk drive exterior, interior, and heads, as required.	**Ac Power-On Checks**
	☐ a. Set AC POWER switch S1 to ON.
☐ f. Check logic boards for proper seating.	☐ b. Blower motor starts. Controller must be powered on or a jumper plug installed in SIGNAL IN connector J3.
Mechanical Checks	
☐ a. Check all latches, covers, and doors for proper operation.	☐ c. Check for signs of possible trouble areas and listen for any audible indications of trouble.
☐ b. Check door-closed, heads-extended, and rack-end microswitches.	**Voltage Checks**
	☐ a. +5 vdc, ±0.050 vdc
☐ c. Check pack-on switch for proper operation.	☐ b. +24 vdc, ±1.2 vdc
☐ d. Check spindle drive belt and tension spring.	☐ c. -24 vdc, ±0.48 vdc
	☐ d. -24 vdc (servo), ±0.48 vdc
Cable Connections	☐ e. +45 vdc, +2.25 vdc, -4.5 vdc
☐ a. Check all cables and receptacles for bent, loose, or recessed pins.	☐ f. +36 vdc, ±1.8 vdc (at 15B53)
	☐ g. +32 vac ±3.2 vac
☐ b. Check all cables for proper length.	**Operational Checks**
☐ c. Install cables.	☐ a. Check for proper installation of disk packs — no mechanical binding, and pack switch closed.
Pre-power On Resistance Checks	☐ b. Check first seek operation.
☐ a. Check for proper ground continuity between chassis and DC COMMON, deck plate, head block, PDP, and pin 3 and 57 of chassis A, B, and C.	☐ c. Check spindle brush resistance for less than one ohm, to ground.
	☐ d. Check servo alignment.
	☐ e. Check read/write head alignment.
	☐ f. Check radial alignment (cylinder 118, head 9 or 10 on CE alignment pack).
☐ b. Check resistance between chassis ground and each dc voltage buss for less than 3 ohms to ground. Check the +5V, -24V, -24V SVO, +24V, +45V, at the power supply, and at 15B53, check for +36 vdc.	☐ g. Check gap scatter if special CDS alignment pack is available with gap scatter information added to cylinder 3, all heads.
	☐ h. Run diagnostic routines.
	☐ i. Assure that customer jobs are executed properly.

VISUAL INSPECTION

When all shipping and packaging materials are removed, inspect the disk drive in the following manner:

a. Inspect all areas for internal or external damage that might have occurred during shipment (see Figure 2-1). If damage is observed, immediately submit a full written report.
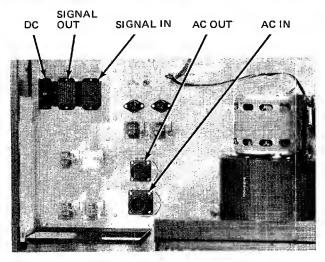
Figure 2-1. Major Subassemblies and Connectors

b. Inspect for proper location and seating of all plug-in modules and relays. Check Equipment Configuration List, inside disk drive, for proper part number and revision levels on logic boards.

c. Check for loose hardware or connections.

d. Inspect all wire-wrap pins for bent or shorted connections.

MECHANICAL CHECKS

The disk drive mechanical checks verify that the pack-on and heads-extended interlocks are positioned and operating properly. Perform a brief mechanical check of the switch interlocks in accordance with procedures in the following paragraphs. Refer to Figure 2-2. If adjustments are required, refer to the appropriate section in this manual.
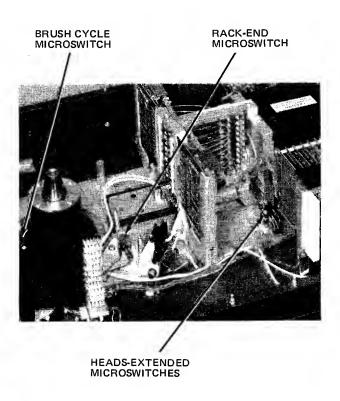
Figure 2-2. Microswitch Locations

PACK-ON SWITCH

a. With disk pack removed, observe that leaf switch contacts (underside of deck plate) are open.

b. Install disk pack.

c. Observe that leaf switch contacts close.

d. Remove disk pack.

HEADS-EXTENDED MICROSWITCHES

a. Manually extend read/write heads ½-inch maximum.

b. Observe that both heads-extended microswitches open, at exactly the same time, after approximately ¼-inch of movement.

c. Retract heads slowly. Observe that both microswitches close, at exactly the same time, within 3/16- to 1/4-inch of fully retracted position.

ON-LINE MICROSWITCH (STANDARD MODEL)

a. Insert unit identifier plug into position and slowly press inward.

b. Observe that on-line microswitch contacts (Figure 2-3) close approximately 1/8-inch before plug is fully seated.

ON-LINE
MICROSWITCH (TYP)
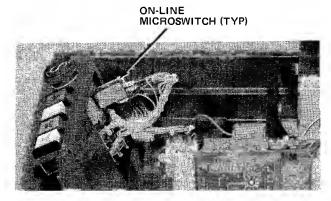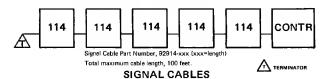
Figure 2-3. On-Line Microswitch Location
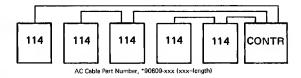
CABLE CONNECTIONS

Ac power, some dc power, control, status, and read/write signals are routed between the controller and the disk drives by three separate cables; ac power cable, dc cable and the signal cable (see Figures 2-4 and 2-5).
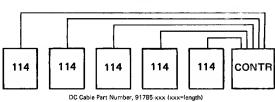
NOTE

Before attempting to connect the system cables, check cable and respective receptacle for possible shipping damage. Special care should be taken to check for bent or recessed connector pins.

Signal Cable Part Number, 92914-xxx (xxx=length)
Total maximum cable length, 100 feet.

⚠ TERMINATOR

SIGNAL CABLES

AC Cable Part Number, *90609-xxx (xxx=length)
Keep total cable lengths under 500 feet.
*50-Hz Part Number, 91552-xxx

AC CABLES

DC Cable Part Number, 91785-xxx (xxx=length)
Maximum cable length, 50 feet.

DC CABLES

Figure 2-5. Connecting Cables

The function and connection point for each connecting cable is listed in Table 2-2.

UNIT NO. 1

UNIT NO. 2

TERMINATOR

DC IN TO UNIT 2
DC IN TO UNIT 2
SIGNAL FROM UNIT 1
AC FROM CONTROLLER
AC FROM CONTROLLER

SIGNAL FROM UNIT 1/SIGNAL TO UNIT 2
AC FROM UNIT 1/AC TO UNIT 2
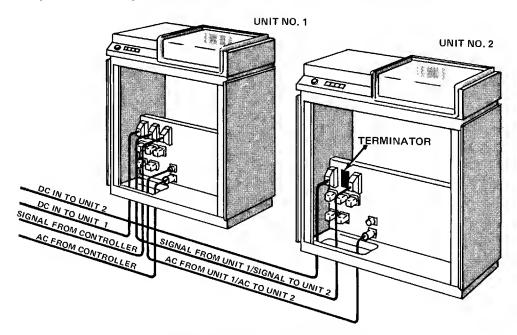
Figure 2-4. Multiple Disk Drive Cable Connections

Table 2-2. Cable Connections

| Cable | Connection | | Function |
	Input	Output	
AC Power	J1 AC IN		Ac input from controller or from preceding cabinet.
		J2 AC OUT	Ac output to next disk drive. Combined lengths of ac power cables in one chain to be 100 feet maximum.
Signal	J3 SIGNAL IN		Control and buss signals input from controller or from preceding cabinet.
		J4 SIGNAL OUT	Control and buss output to next cabinet or terminated in the last cabinet (use terminator supplied). Combined lengths of all signal cables to be 100 feet maximum.
Dc	J5 DC		Read/write data, some dc power, and status input direct from controller to each disk drive. Maximum length of each dc cable to be 50 feet.

AC POWER CABLE

The disk drive operates on 208 or 230 vac, single-phase, 60 Hz power (50 Hz optional). For multiple disk drive operation the ac power cable connects three-phase ac power from the controller to the first, third, and fifth cabinet. In order to maintain phase-to-phase load balance, each input phase is rotated for succeeding disk drives (see Table 2-3 and Figure 2-6).

All other cabinets are connected, in daisy chain fashion, to AC OUT connector J2 of the preceding cabinet.

Table 2-3. Ac Power Cable

Pin	Line Name	Wire Size
A	208 vac	#12
B	208 vac	#12
C	208 vac	#12
*D	Neutral	#12
G (GND)	Ground	Shield
*50 Hz only		

DC CABLE

A dc cable is connected from the controller to each disk drive. Each dc cable carries the read/write data, certain isolated control signals, and optional logic levels for each disk drive. Refer to Table 2-4.
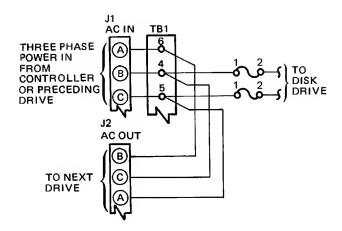
Figure 2-6. Three-Phase Ac Connections

Route both dc cables up through the cable access channel and connect to DC UPPER and DC LOWER connectors J5.

Table 2-4. Dc Cable

| Signal Pin | | Ground Pin | | Signal Name |
STD	OEM	STD	OEM	
27	3	-	-	Dc Ground *10
-	5	*	*	Write Data Coaxial
-	12	*	*	Read Data Coaxial
-	14	-	-	+3 v (Q Logic Level)
12	17	-	-	Read/Write Data Coax
02	19	-	-	-3 v (Q Logic Level)
-	21	-	26	Gated Attention
22	22	27	27	Selected Module
-	23	-	28	Module Selected
*Grounded in Cable Plug Module 02B				

SIGNAL CABLE

A signal cable is connected from the controller to the first disk drive SIGNAL IN connector J3. Each succeeding disk drive receives the signal cable input from SIGNAL OUT connector J4 of the preceding unit. The last unit must have a signal terminator installed in SIGNAL OUT connector J4.

Route the signal cable up through the cable access channel and connect to SIGNAL IN connector J3.

Figure 2-7 shows the location of SIGNAL OUT connector J4, pin A (in standard units with a 104-pin connector) or pin 1 (in OEM units with 75-pin connectors). Refer also to Table 2-5.
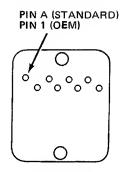
Figure 2-7. First Pin Location, Connector J4

TERMINATOR

A terminator assembly is installed in SIGNAL OUT connector J4 of the last drive.

Up to nine drives can be connected to one controller; eight drives for on-line operation, and one spare.

POWER SUPPLY CHECKS

ISOLATION CHECKS

Isolation checks are made to ensure that a voltage bus is not shorted to ground and that good grounding has been maintained. See Figure 1-8 and Table 2-6 and perform

power supply isolation checks in accordance with Table 2-6.

NOTE

On earlier model units, the physical location of the dc voltage terminals differs from that shown in Figure 2-8.
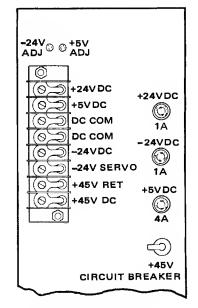
Figure 2-8. Dc Power Supply

Table 2-5. Signal Cable

Signal Pin		Ground Pin		Signal Name
STD	OEM	STD	OEM	
A	1	B	2	Drive Bus 0
C	3	D	2	Drive Bus 1
E	4	F	5	Drive Bus 2
H	7	J	5	Drive Bus 3
K	8	L	10	Drive Bus 4
M	11	N	10	Drive Bus 5
P	12	R	13	Drive Bus 6
S	14	T	13	Drive Bus 7
U	15	V	16	Set Difference Tag
W	17	X	16	Set Cylinder Tag
Y	18	Z	20	Set Head and Direction Teg
a	21	b	20	Control Tag
-	24	-	23	Clock Out
AX	40	AY	41	Cylinder Address Register 0 (1)
AZ	42	BA	41	Cylinder Address Register 1 (2)
BB	43	BC	44	Cylinder Address Register 2 (4)
BD	45	BE	44	Cylinder Address Register 3 (8)
BF	46	BH	47	Cylinder Address Register 4 (16)
BJ	48	BK	47	Cylinder Address Register 5 (32)
BL	49	BM	50	Cylinder Address Register 6 (64)
BN	51	BP	50	Cylinder Address Register 7 (128)
CD	67	CE	66	Read Only
-	52	-	53	Selected Drive Ready
BT	54	BU	53	Selected On-line
BV	55	BW	56	Selected Index
BX	57	BY	56	Selected Drive Unsafe
BZ	58	CA	59	Selected Seek Error
BR	-	BS	-	Selected Drive Busy
CB	60	CC	59	Selected End of Cylinder

Signel Pin		Ground Pin		Signal Name
STD	OEM	STD	OEM	
-	62	-	63	Selected Sector
CF	64	CH	63	Selected Write Current Sensed
CJ	65	-	66	Heads Extended
-	32	-	23	CPU Helt
CK	76	-	-	Controlled Ground
CL	78	-	-	+36 v Out
CM	77	-	-	+36 v Sequence Pick In
-	79	-	-	Terminator -3 v dc
-	80	CR	-	Shield Ground
-	82	-	-	Shield Ground
AT	-	CS	-	+5 v (D Logic Level)
c	-	d	-	Module 0 Select
f	-	g	-	Module 1 Select
h	-	d	-	Module 2 Select
j	-	k	-	Module 3 Select
m	-	n	-	Module 4 Select
p	-	q	-	Module 5 Select
r	-	s	-	Module 6 Select
t	-	u	-	Module 7 Select
v	-	w	-	Spare Module Select
x	-	y	-	Gated Attention from Module 0
z	-	AA	-	Geted Attention from Module 1
AB	-	AC	-	Gated Attention from Module 2
AD	-	AE	-	Gated Attention from Module 3
AF	-	AH	-	Gated Attention from Module 4
AJ	-	AK	-	Geted Attention from Module 5
AL	-	AM	-	Gated Attention from Module 6
AN	-	AP	-	Gated Attention from Module 7
AR	-	AS	-	Gated Attention from Spare Module

Table 2-6. Power Supply Resistance Checks

From	To
+24V	PDP Chassis
+5V	Dc COM
-24V	Chassis A, B, and C, pins 3 and 57
-24V SERVO	Dc COM
+45V	Deck Plate
+36 vdc (15B53)	Head Block Assy
All measurements should be 3 ohms or greater.	

INPUT AC POWER

Check the ac input power between any two phases to determine the magnitude of the available ac power. After ac power is applied, it can be measured at the main power input connector or at AC OUT connector, pins A, B and C of any cabinet.

WARNING

Care should be taken when measuring or connecting the input ac power. Set AC POWER switch S1 to OFF when connectors are being made to power leads.

If the input ac power is between 190 vac and 218 vac connect the power supply voltage input to TB1-4 (208 vac), see Figure 2-9.

If the input is between 219 vac and 253 vac, connect the input to TB1-3 (230 vac). For this connection the line frequency (50 or 60 Hz) is not a consideration.

NOTE

On earlier model units, the physical location of the ac voltage terminals differs from that shown in Figure 2-9.
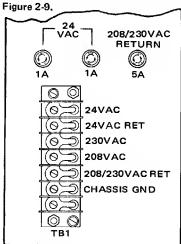
Figure 2-9. Ac Voltage Terminals

AC POWER-ON CHECKS

NOTE

If the disk drive is not connected to the controller +36V SEQ PICK IN and CGND are derived internally by jumpering +36V OUT (J3-CL) to +36V SEQ PICK IN (J3-CM) and CGND (J3-CK) to ground (J3-CP).

After the input ac power has been applied to the system (power switch on), perform the following:

a. Observe that disk drive blower is on, supplying filtered air to air shroud (disk pack compartment).

b. Check that there are no visible or audible signs of electrical shorts.

VOLTAGE CHECKS

Check the voltages before attempting any disk drive operation. The +5 volts is adjustable. If any other voltage is not within tolerance the power supply may have to be replaced. The +36 volts is generated from the +45 volts. Check all voltage levels as listed in Table 2-7. Refer to Figures 2-8 and 2-9 for terminal locations.

Table 2-7. Power Supply Voltage Checks

Voltage Terminals		Ground Terminal
+5V	(±50 mvdc, adjustable)	
+24V	(±1.2 vdc)	
-24V	(±0.48 vdc)	
-24V SVO	(±0.48 vdc)	DC COM
+45V	(+2.25, -4.5 vdc)	
+36 vdc	(±1.8 vdc, at 15B53)	
24 vac	(±2.4 vac)	24 VAC RET

OPERATIONAL CHECKS

DISK PACK LOADING

The disk pack should mount onto the spindle assembly without mechanical binding. If binding does occur, remove the disk pack and clean the spindle cone and the recessed screw mechanism with a cotton swab, lightly dampened with 91 percent isopropyl alcohol.

FIRST SEEK CHECKS

During the first seek operation, several visual and audible checks can be made. After the disk pack has been installed, press the power-on pushbutton on the control panel and observe the following events:

a. Disk pack starts to rotate; brush assemblies move into disk pack area at approximately same time.

b. Approximately 4 seconds after disk pack starts rotating, centrifugal switch in spindle drive motor audibly switches to high speed run position.

c. Observe that brushes move into disk pack and then retract. Brushes must be completely retracted from disk pack before read/write heads start to move forward. If not, adjust brush assembly microswitch.

CAUTION

Check that brushes are centered between disk surfaces. Brushes will burn if not evenly located.

d. Head carriage moves forward to end stop and reverses to return heads to cylinder 000.

SPINDLE GROUNDING BRUSH RESISTANCE

While disk pack is rotating at full speed, check resistance between spindle grounding brush and fixed contact arm of pack switch. Resistance must be less than 1 ohm. If not, clean point of contact on contact arm with fine emery cloth (see Figure 2-10).
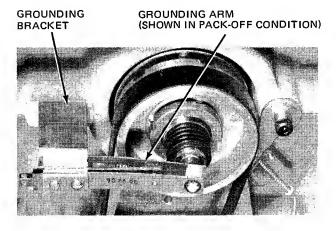
Figure 2-10. Spindle Brush and Pack-On Switch

SERVO SYSTEM ALIGNMENT CHECKS

The servo system must be checked to assure proper positioning of the read/write head assemblies to the desired cylinder, and the proper detenting (electronic locking) at that cylinder.

The following procedures are provided to check and adjust a normally operating disk drive servo system. If problems are encountered during alignment, refer to Section 5 of this manual for a more detailed checkout.

Figure 2-11 shows the servo adjustment locations. If the disk drive controller does not have the features necessary to operate the drive off-line, the disk drive exerciser must be used (Figure 2-12).
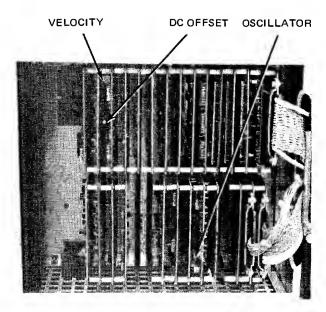
Figure 2-11. Oscillator and Servo Adjustment Locations
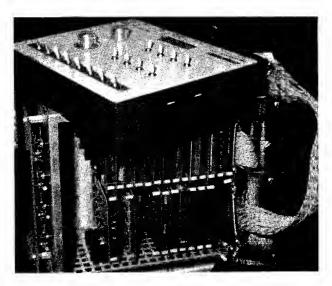
Figure 2-12. Disk Drive Exerciser Installed

OSCILLATOR

a. Check 100 kHz oscillator voltage at 06B01 for peak-to-peak amplitude of 5 ±0.2 volts.

b. Observe that amplitude is 2.5 volts above ground and 2.5 volts below ground. Amplitude may be adjusted with oscillator potentiometer.

DEMODULATOR NULL AND SERVO OFFSET

a. While performing a one-cylinder alternate seek, with approximately 40 milliseconds between seeks, check servo offset for single waveshape, and demodulator null for minimum amplitude (see Figure 2-13).

PROG: Repetitive Single Cylinder Seeks

SYNC: Ext   AC   5 µs 06B01   100 KHZ OSC

CHAN: 1   AC   50 mv 05C04   CYLXDUCER;S

MODE: CHAN 1 only

NOTE: Null period between seeks — 40 milliseconds
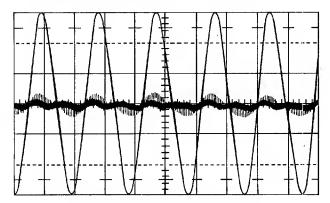
Figure 2-13. Servo Adjustment Waveform

b. If necessary alternately adjust SERVO NULL and DC OFFSET potentiometers for best results.

POSITION GAIN

a. Perform seek operations of one cylinder forward, one cylinder reverse, 203 cylinders forward, and 203 cylinders reverse.

b. Observe, at GTDATN/ time, signal amplitude is less than 130 millivolts in all cases. If not, adjust POSITION GAIN potentiometer for best compromise less than 130 millivolts. Refer to Figures 2-14 and 2-15.

PROG: Repetitive Single Cylinder Seeks
SYNC: *Ext +DC   2 ms   09A05   SKFWD
CHAN: 1   AC   100 mv 05C04   CYLXDUCER;S
CHAN: 2   +DC   5 v   11A30   GTDATN/
MODE: Added
NOTE: GTDATN/ = Seek Complete
*For reverse: Ext   -DC   2 ms   09A05   SKFWD
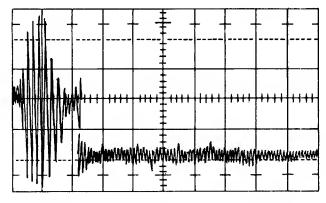
Figure 2-14. Cylinder Transducer Output, 1 Cylinder Seek

PROG: Full 203 Cylinder Seek
SYNC: *Ext +DC   100 ms 09A05   SKFWD
CHAN: 1   AC   100 mv 05C04   CYLXDUCER;S
CHAN: 2   DC   5 v   11A30   GTDATN/
MODE: Added
NOTE: GTDATN/ = Seek Complete
*For reverse: Ext   -DC   100 ms   09A05   SKFWD
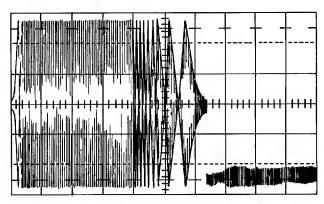
Figure 2-15. Cylinder Transducer Output, 203 Cylinder Seek

VELOCITY

a. Check velocity for 65 milliseconds from beginning of seek operation to GTDATN/ time (Refer to Figure 2-15).

b. Observe that transducer output at GTDATN/ time is less than 130 millivolts; if not, recheck position gain adjustment, and adjust VELOCITY potentiometer, as required.

CYLINDER TRANSDUCER

a. Check that amplitude of cylinder transducer envelope is 600 millivolts minimum and 1.5 volts maximum, peak-to-peak (800 millivolts nominal).

b. Observe that amplitude does not vary more than 400 millivolts peak-to-peak from end to end.

c. Observe that any two adjacent envelopes do not have an amplitude variation greater than 20 percent, peak-to-peak.

READ/WRITE HEAD ALIGNMENT CHECKS

Read/write head alignment is checked to ensure that a disk pack written on one drive can be read by other compatible drives. Alignment should not be attempted unless the temperature of the disk drive and alignment disk pack is stabilized.

HEAD ALIGNMENT

a. Install an alignment disk pack and disk drive exerciser.

b. Remove write driver from location 03C.

c. Program exerciser to perform a READ on head 00 at cylinder 73.

d. Monitor read data playback (Figure 2-16).

PROG: Read CE Cylinder 73
SYNC: Ext   +DC   2 ms*   03A30   INDEX
CHAN: 1   AC   200 mv   02C13   READ DATA
CHAN: 2   AC   200 mv   02C15   READ DATA/
MODE: CHAN 2 inverted and added

*Adjust vernier sweep uncalibrated for one full "Cat Eyes" waveform (1 Revolution — 10 cm = 25 ms).
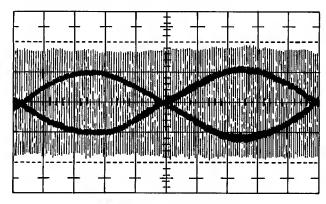
Figure 2-16. "Cat Eyes" Waveform

e. With oscilloscope in uncalibrated position, adjust sweep to display two complete lobes with ends of lobes at each end of graticule.

f. Observe that all crossovers occur at ±4 minor divisions from center graticule and that all heads are within ±2 minor divisions of the average crossover point.

g. Adjust read/write head, if necessary, to align all heads within one minor division of the average crossover point.

PROXIMITY CHECK

a. Remove air shroud.

b. Install a scratch pack.

c. Install a 0.033-inch feeler gauge between sector/index transducer and disk pack (Figure 2-17).

NOTE

In step d the allen screw must touch transducer mount while check is being made.

d. Check for slight pack drag.

e. If necessary turn adjusting screw until slight drag is felt.
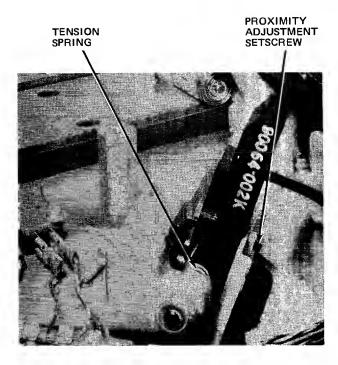
Figure 2-17. Sector/Index Transducer Adjustment

RADIAL ALIGNMENT

The radial alignment check is a position check for the sector/index transducer. The check is made to ensure that when the index pulse occurs, the read/write heads and the data field of the disk pack are both in the correct angular position.

a. Observe that first pulse is 3 ±2 microseconds from index pulse (start of sweep, Figure 2-18) and that burst of data pulses starts 5 (+1, -0) microseconds from first pulse.

PROG: Read CE Cylinder 118 Head 9 or 10
SYNC: Ext   +DC   1 µs   03A30   INDEX
CHAN: 1   AC   100 mv   02C13   READ DATA
CHAN: 2   AC   100 mv   02C15   READ DATA/
MODE: CHAN 2 inverted and added

Figure 2-18. Radial Adjustment Waveform
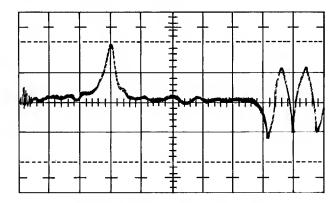
b. To adjust for radial alignment, observe waveform (Figure 2-18) of either head 9 or 10, and adjust radial adjustment locknut of index transducer.

c. Recheck proximity adjustment.

GAP SCATTER

This alignment check can only be made if the CDS alignment pack to be used has had the gap scatter information added to cylinder 3 and 201, all tracks. If the information has been added, the top of the pack will be labeled.

a. While reading CE alignment pack cylinder 3, record time from start of sweep (INDEX) to data burst for all heads.

b. Observe that time to data burst is approximately 10 microseconds, and all heads are within 8 microseconds of each other (see Figure 2-19).

PROG:	Read CE Cylinder 3, All Heads				
SYNC:	Ext	+DC	2 μs	03A30	INDEX
CHAN:	1	AC	100 mv	02C13	READ DATA
CHAN:	2	AC	100 mv	02C15	READ DATA/
MODE:	CHAN 2 inverted and added				
NOTE:	Replace heads out of tolerance				
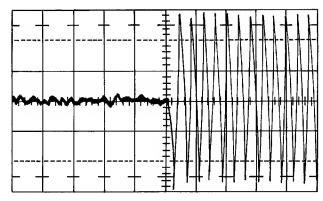
Figure 2-19. Gap Scatter Waveform

DIAGNOSTIC ROUTINES

Run all available diagnostic routines. The routines must run error free. If trouble is encountered during testing, refer to the Maintenance section of this manual.

CUSTOMER PROGRAMS

The final check for the disk drive is the proper execution of all customer programs (jobs). If the disk system is new and the customers jobs have not been completely debugged, there is a possibility of software problems. The systems analyst should be notified.

SECTION 3

THEORY OF OPERATION

GENERAL

This section provides a comprehensive theory of operation and is divided into the following subsections:

- Functional Description
- Power Sequencing
- Positioning System
- Read/Write System
- Error Detection
- Communications

LOGIC CONVENTIONS AND SYMBOLOGY

The Model 114 Disk Drive uses 5-Volt Diode Transistor Logic (5VDTL) where a voltage more positive than +2.2 volts (turn-on threshold) is considered as a logical high and a voltage more negative than 1.7 volts (turn-off threshold) is considered as a logical low. Figure 3-1 shows the logic high and low ranges.
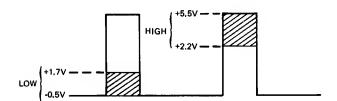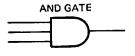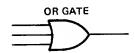
Figure 3-1. Logic Levels

The following conventions are provided to aid in understanding the symbology used in this manual.

AND GATE
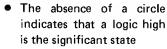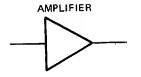
- The output is high if and only if all inputs are high

OR GATE

- The output is high if any input is high

AMPLIFIER

- A circle placed adjacent to a logic symbol indicates that a logic low is the significant state
- The absence of a circle indicates that a logic high is the significant state
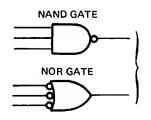
- If any input is active the output is active

LOGIC SYMBOLOGY
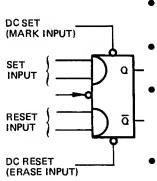
The following logic symbology is used throughout this manual:

NAND GATE

NOR GATE

- If all inputs are high, the output is low, conversely
- If any input goes low, the output goes high

JK FLIP-FLOP
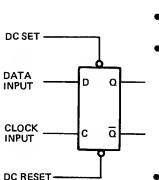
- If the DC SET (MARK) input goes low, the flip-flop sets
- If the DC RESET (ERASE) input goes low, the flip-flop resets
- If both SET INPUTS are high and the clock goes low the flip-flop sets, provided MARK and ERASE are high
- If both RESET INPUTS are high and the clock goes low the flip-flop resets, provided MARK and ERASE are high.
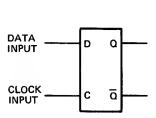
POSITIVE EDGE TRIGGERED D-TYPE FLIP-FLOP
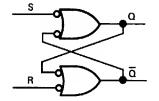
- If DC SET input goes low, latch sets
- If DC RESET input goes low, latch resets
- When CLOCK INPUT GOES FROM LOW TO HIGH transition, flip-flop latches to state of DATA INPUT, provided DC SET and DC RESET are both high
- When CLOCK INPUT goes from a high to low transition, flip-flop remains latched

NEGATIVE EDGE TRIGGERED D-TYPE FLIP-FLOP
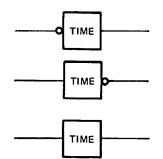
- When CLOCK INPUT goes from low to high transition, Q output follows DATA INPUT, and $\overline{Q}$ output is complement of DATA INPUT and Q output
- When CLOCK INPUT goes from high to low transition, flip-flop latches to state of DATA INPUT

CROSS COUPLED LATCH
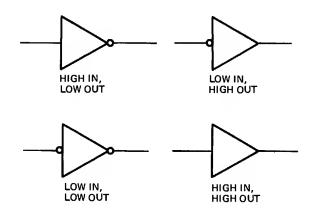
- When S input goes low latch sets
- When R input goes low latch resets

ONE SHOT, HOLDOVER CIRCUITS
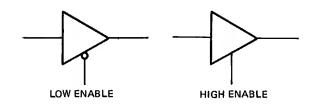
- When input goes low, output goes high for time shown inside box
- When input goes high, output goes low for time shown inside box
- When input goes high, output goes high for time shown inside box
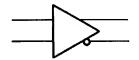
LINE RECEIVER, LINE DRIVER, ANALOG SWITCH, AMPLIFIER, RELAY DRIVER, LAMP DRIVER

HIGH IN, LOW OUT

LOW IN, HIGH OUT

LOW IN, LOW OUT

HIGH IN, HIGH OUT

TRANSISTORS

LOW ENABLE

HIGH ENABLE
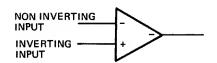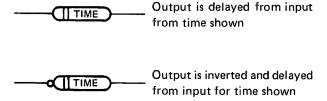
DIFFERENTIAL AMPLIFIER

OPERATIONAL AMPLIFIER

NON INVERTING INPUT

INVERTING INPUT

TIME DELAYS

TIME — Output is delayed from input from time shown

TIME — Output is inverted and delayed from input for time shown
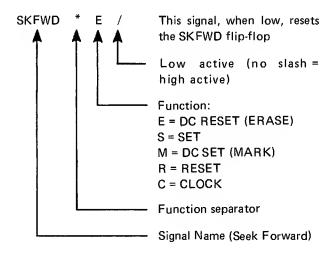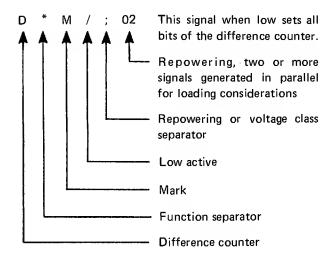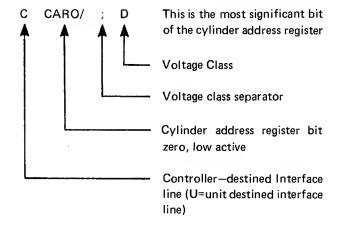
LOGIC MNEMONICS AND FUNCTION DESIGNATORS

The following are three examples of logic mnemonics and function designators:

SKFWD   *   E   /

This signal, when low, resets the SKFWD flip-flop

Low active (no slash = high active)

Function:
E = DC RESET (ERASE)
S = SET
M = DC SET (MARK)
R = RESET
C = CLOCK

Function separator

Signal Name (Seek Forward)

D   *   M   /   ;   02

This signal when low sets all bits of the difference counter.

Repowering, two or more signals generated in parallel for loading considerations

Repowering or voltage class separator

Low active

Mark

Function separator

Difference counter

C   CARO/   ;   D

This is the most significant bit of the cylinder address register

Voltage Class

Voltage class separator

Cylinder address register bit zero, low active

Controller—destined Interface line (U=unit destined interface line)

FUNCTIONAL DESCRIPTION

Figure 3-2 is a block diagram of the disk drive and provides a brief description of each major drive element.
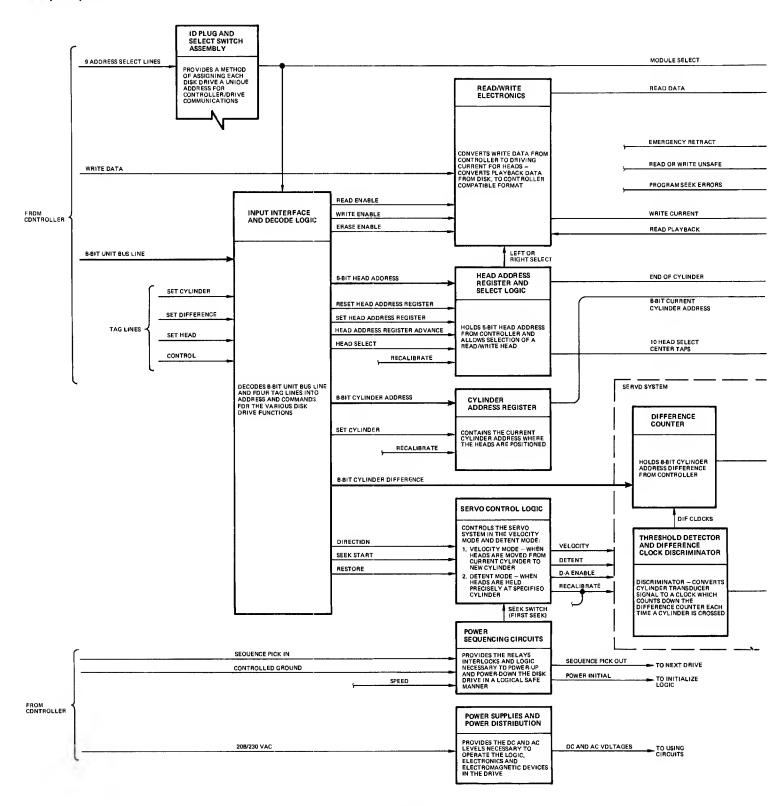
Figure 3-2. Model 114 Block Diagram (sheet 1 of 2)

Figure 3-2. Model 114 Block Diagram (sheet 2 of 2)
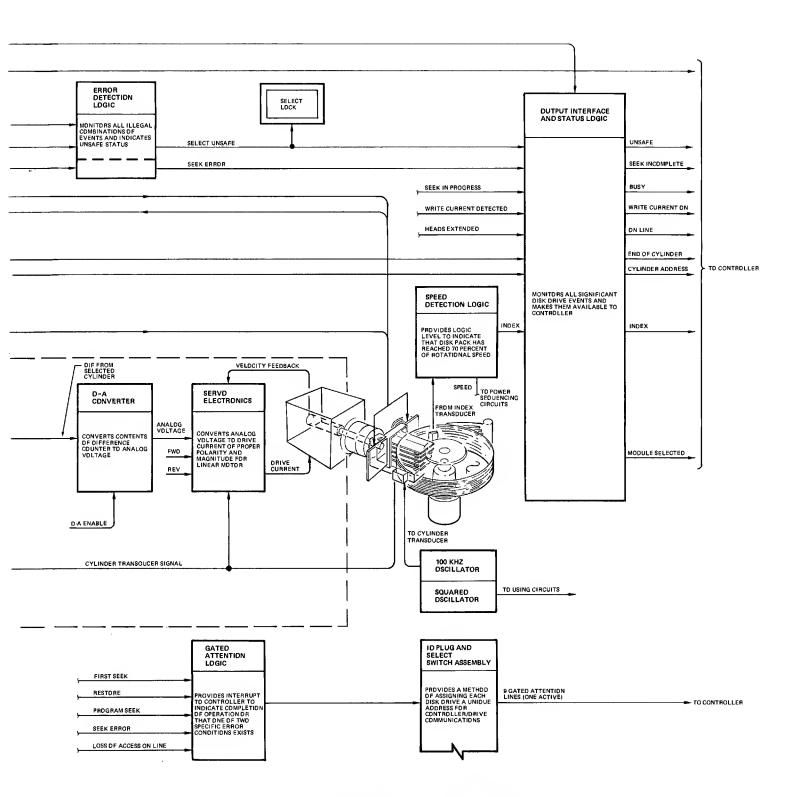
Disk drive operation can be divided into the following functional sequences:

- Power Up
- First Seek
- Program Seek
- Read/Write
- Power Down

The following paragraphs provide a general description of each mode of operation.

POWER-UP

The power up sequence allows each drive to be powered-up separately to prevent drawing starting current on several disk drive motors at the same time.

To initiate a power-up sequence, power is applied to the controller. The controller then supplies 3-phase ac power to all drives in the system. Each drive uses only two phases of the 3-phase power and phases are rotated between drives to balance the load.

A Sequence Pick In voltage is then connected from the controller to the first drive in the line. In addition, the controller supplies a Controlled Ground level to all drives. These two levels are used to energize a power-sequence relay in each drive.

Sequence Pick In provides the +24 volts for the sequence relay and controlled ground is the ground return line for the relay.

If the AC POWER switch is OFF in the first drive, Sequence Pick In is bypassed to the next drive to start the power-up sequence for that drive.

Normally the AC POWER switch is left ON. If the AC POWER switch is ON, ac power is applied to the dc power supplies and to the air system blower motor, and a logic initialization pulse is developed to initialize critical logic.

If a disk pack is installed, the disk pack access door closed, and the POWER ON switch is on, ac power is applied to the disk pack drive motor and to the disk pack brush cleaning motor. The disk pack begins to rotate and a cleaning brush sweeps across each disk surface to remove dust and particles which could cause head/disk damage or data errors.

When the disk pack reaches approximately 1680 rpm, speed detection logic causes a power sequencing relay to send Sequence Pick Out to the next drive as Sequence

Pick In for that drive. This is performed to start the power-up sequence in the next drive.

As the cleaning brushes move to their retracted position, a latch sets in the power-up circuits, and the servo control logic is initialized to start the first-seek operation.

FIRST SEEK

The purpose of the first-seek operation is to "load the heads" onto the air-bearing formed by the rotating disk pack and then to position the heads at cylinder 000.

The first-seek operation begins when the brush cycle is complete and the disk pack has reached 70 percent of its rotational speed.

Upon achieving the two conditions the following occurs:

- The servo control logic develops a recalibrate signal which causes the servo system to drive the head carriage to the end of its travel. This then loads the heads
- The head carriage is then driven in reverse at high speed to cylinder 000 and the servo control logic enters the detent mode to hold the read/write heads precisely at cylinder 000
- The gated attention logic develops an interrupt to indicate the first seek operation is complete
- The status logic holds the present status of the drive in anticipation of the drive being selected

ADDRESSING AND SELECTING A DISK DRIVE

To address a disk drive an ID plug must be installed in the receptacle provided in the operator control panel.

The ID plug provides the means of giving each drive a unique identity. When the ID plug is installed, it causes one of nine ID select switch position to close. Each select switch position is connected to one of nine address lines from the controller.

When the controller selects a drive one of nine address lines are active to all drives in the system. The drive with the ID select switch closed and corresponding address line active is then selected.

When the drive is selected the input and output interface logic is enabled and the following occurs:

- A module selected signal is sent to the controller
- The disk drive status is presented to the controller
- The current cylinder address is presented to the controller

If the selected drive is not safe for operation, error detection logic disables the input and output interface and an unsafe signal is sent to the controller.

POWER SEQUENCING

The power sequencing circuits provide the means of sequentially controlling disk drive power-up and power-down functions. The main objectives of the power sequencing circuits are to:

- Establish conditions to perform a first seek as a result of power-up

- Remove read/write heads from rotating disk pack as a result of power-down

The power-up and power-down sequences are controlled by sequence relays and switch interlocks located on the power distribution panel (PDP), deck plate, and operator's control panel. The power sequencing circuits control the dc power supply blower motor, disk pack drive motor, and brush cycle motor. Logic is provided to generate index pulses, detect disk pack rotational speed and initiate first seek as a result of power-up.

The objective of the power-up sequence is to perform the following tasks:

- Develop dc operating voltages

- Start blower motor

- Determine if interlocks are closed

- Start and maintain disk drive motor rotation

- Clean disk pack by cycling brush motor

- Develop index pulses and detect disk pack rotational speed

- Transfer power-up sequence voltage to next drive

- Establish initial conditions for first seek

The disk drive can be operated in a system configuration (i.e., connected to a controller) or as a stand-alone unit.

SYSTEM POWER-UP SEQUENCE

The following is required from the controller for a system power-up sequence:

- +36v relay sequencing voltage (+36V SEQ PICK IN)

- Controlled ground (CGND)

- 208/230-volts, 3-phase, 50 or 60 Hz ac power

AC Power Application

To initiate a power-up sequence, the controller supplies 208/230-volts, 3-phase, 60Hz ac power (50Hz optional) in parallel to all drives. Each drawer uses only two phases of the three phase power, and phases are rotated between drawers as well as between drives to balance line power. Figure 3-3 shows the ac power distribution.

The phases are rotated by the J1 and J2 wiring. Ac power is applied to terminal board TB1. If AC POWER switch S1 is closed, ac power is applied through line filter FL1 to the dc power supply, Drive Motor relay K5 contact, and Blower relay K2 contact.
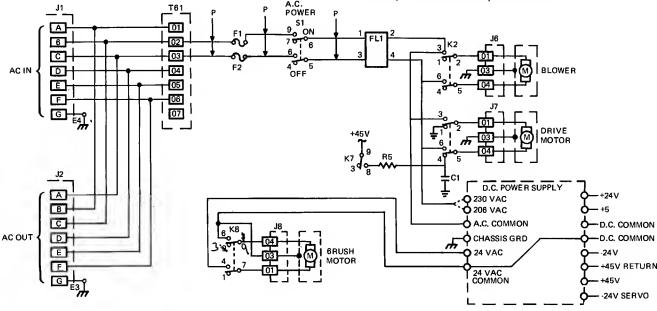
Figure 3-3. Ac Power Distribution

Logic Initialization

The logic initialization circuit (Figure 3-4) comprises an RC time constant and two gates. Upon ac power application, the +5 volt supply energizes. PWRINI goes high, PWRINI/ goes low and C4 begins charging towards +5 volts. Approximately 25 milliseconds after power application, C4 charges to +2 volts, PWRINI goes low, and PWRINI/ goes high: thus a 25 millisecond logic

initialization pulse is developed.

PWRINI/ and PWRINI erase the following flip-flops:

- Seek enable (SKENA)

- Up to speed (SPEED)

- Drive on line (ON LINE)

- Attention (ATTEN)
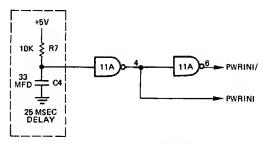
Figure 3-4. Initial Power

Figures 3-5 through 3-11 describe each phase of the system power-up sequence:

- Figure 3-5. Routing +36V Sequence Pick Voltage to Next Drive
- Figure 3-6. Energizing Drive Motor Relay K5
- Figure 3-7. Energizing Brush Motor Relay K8 and Speed Relay K5
- Figure 3-8. Energizing Sequence Pick Out Relay K6 and Speed Relay K4
- Figure 3-9. Completing Brush Cycle and Initializing First Seek
- Figure 3-10. Moving Carriage During First Seek
- Figure 3-11. System Power-Up Flow Diagram

ROUTING +36V SEQUENCE PICK VOLTAGE TO NEXT DRIVE

After the dc power supplies stabilize the following occurs:

- The controller applies CGND to all drives in the system, thereby grounding one side of sequence relay K1
- The controller provides SEQUENCE PICK IN (+36V) to energize sequence relay K1 of the first drive in the system
- K1 being energized applies +24 volts to one side of Sequence Pick Out relay K6

The +36 volts (SEQUENCE PICK OUT) is routed to the next drive if any of the following conditions exist:

- AC POWER switch OFF
- AC POWER switch ON and ON/OFF switch OFF
- Disk pack access door open

If the AC POWER switch is OFF, SEQUENCE PICK IN is routed to next drive through AC POWER switch OFF contacts as shown in Figure 3-5 (sheet 1 of 3).
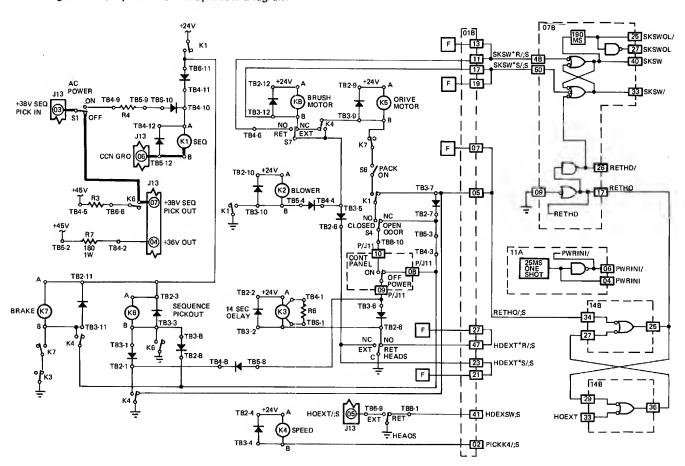
Figure 3-5. Routing +36V Sequence Pick Voltage to Next Drive (sheet 1 of 3)

ROUTING +36V SEQUENCE PICK VOLTAGE TO NEXT DRIVE (continued)

- If AC POWER switch is ON (K1 energized) and the control panel ON/OFF switch is OFF;

Sequence Pick Out relay K6 energizes and SEQUENCE PICK OUT is routed to the next drive
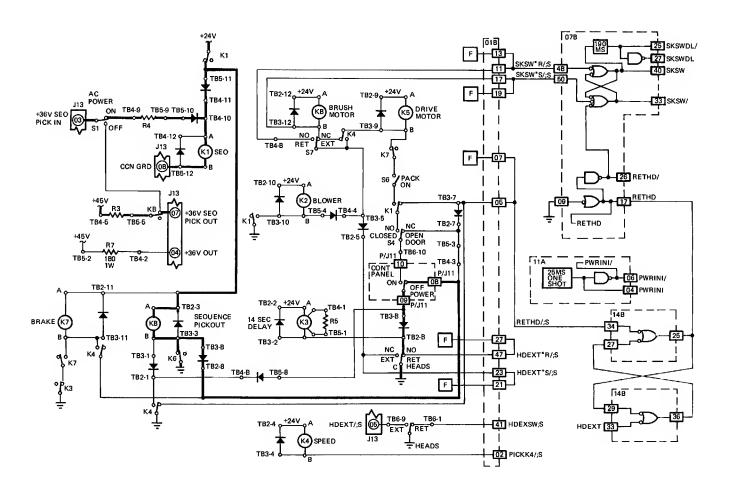
Figure 3-5. Routing +36V Sequence Pick Voltage to Next Drive (sheet 2 of 3)

ROUTING +36V SEQUENCE PICK VOLTAGE TO NEXT DRIVE (continued)

- If disk pack access door is open, Sequence Pick Out relay K6 energizes and Sequence Pick Out is routed to next drive
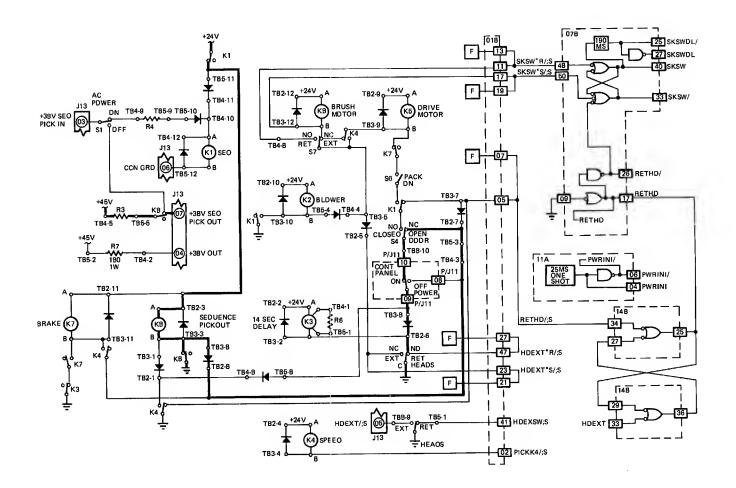
Figure 3-5. Routing +36V Sequence Pick Voltage to Next Drive (sheet 3 of 3)

ENERGIZING BLOWER RELAY K2

The following conditions must be satisfied to energize Blower Relay K2:

- +36 SEQPICKIN relay K1 energized
- Relay K1 contacts must close

With K1 energized the closed contacts of Blower Relay K2 (see Figure 3-3) provide ac power to the blower.
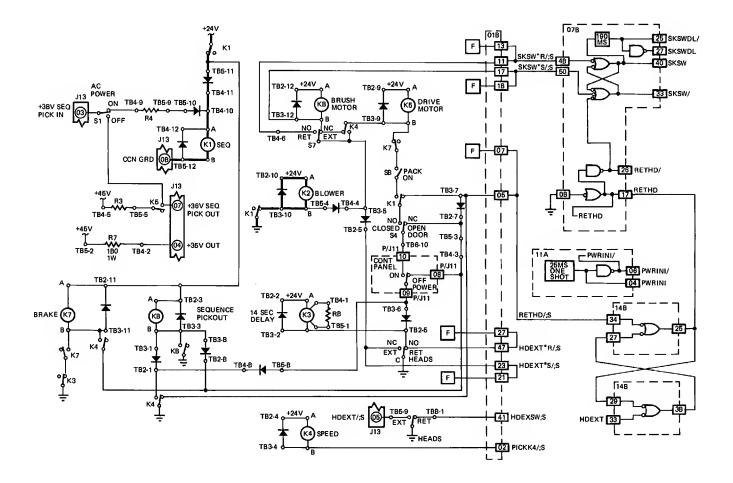
Figure 3-6. Energizing Blower Relay K2

ENERGIZING DRIVE MOTOR RELAY K5

The following conditions must be satisfied to energize Drive Motor Relay K5:

- Brake Relay K7 must be deenergized
- A disk pack must be installed to close the Pack On switch

- The disk pack access door must be closed to close the door closed switch
- The ON/OFF switch must be placed to ON
- K1 must be energized
- Heads must be retracted

The then closed contacts of Drive Motor Relay K5 (Figure 3-3) provide ac power to the disk drive motor.
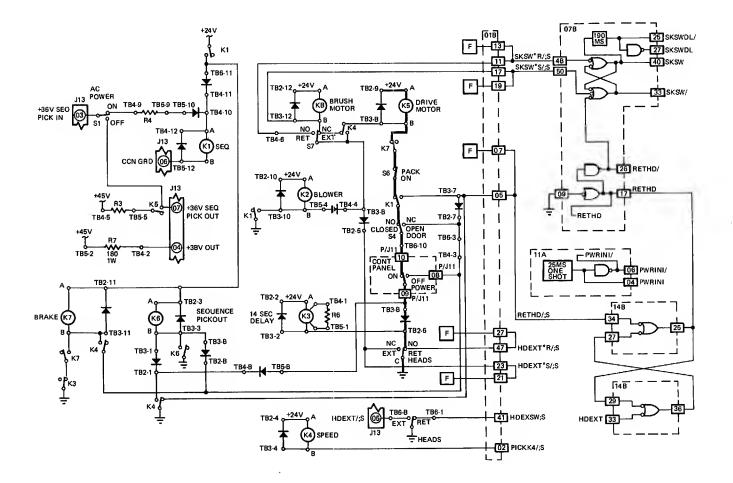
Figure 3-7. Energizing Drive Motor Relay K5

ENERGIZING BRUSH MOTOR RELAY K8 AND SPEED RELAY K4

The power-up sequence continues and the following events occur:

- The same series ground path in conjunction with K4 relay contacts cause Brush Motor relay K8 to energize and reset the seek switch latch (SKSW)
- The closed contacts of relay K8 (Figure 3-3), provide ac power to the brush motor and the disk pack cleaning cycle starts

- The disk drive motor rotates the disk pack, and the index transducer supplies index pulses to the speed detection logic

The speed detection logic provides an enabling signal (PICK K4/;s) after the disk pack rotation gains approximately 70 percent of normal operating speed.

PICK K4/;s energizes speed relay K4.
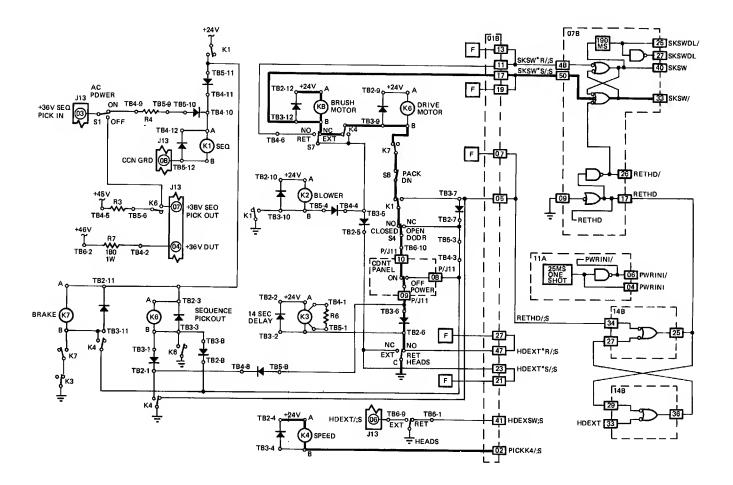
Figure 3-8. Energizing Brush Motor, Relay K8 and Speed Relay K4

ENERGIZING SEQUENCE PICK OUT RELAY K6

The power-up sequence continues and the following events occur:

- Sequence Pick Out relay K6 energizes through K4 contacts. K6 contacts provide an internally developed +36V SEQUENCE PICK OUT signal that is used as SEQUENCE PICK IN to the next drive

- When K4 energized, ground was removed from the RETHD gates. RETHD/ goes high and RETHD goes low thereby initializing the first seek logic
- Approximately 22 seconds after the drive motor and brush motor start, the disk pack surface is swept clean and the brush tower returns to the retracted position
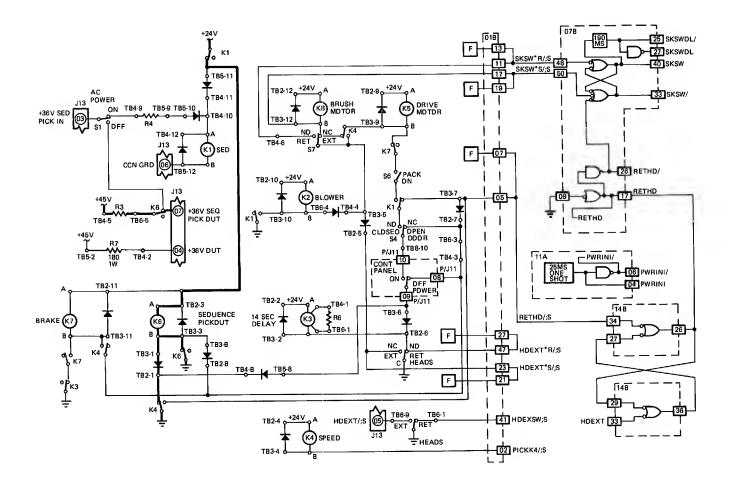
Figure 3-9. Energizing Sequence Pick Out Relay K6

COMPLETING BRUSH CYCLE AND INTIALIZING FIRST SEEK

When the brushes are fully retracted, the brush microswitch opens and the following events occur:

- The ground path for K8 opens when the brush switch transfers from EXT to RET contacts
- When K8 deenergizes, the 32 vac opens to the brush motor and turns the brush motor off

- The new ground path through RET contacts causes SKSW*R/S to go low, setting the seek switch latch (SKSW)
- When SKSW sets, the first seek operation starts
- SKSWDL/ goes high and SKSWDL goes low for 190 milliseconds. The head carriage must clear the heads extended switches within the 190-millisecond window
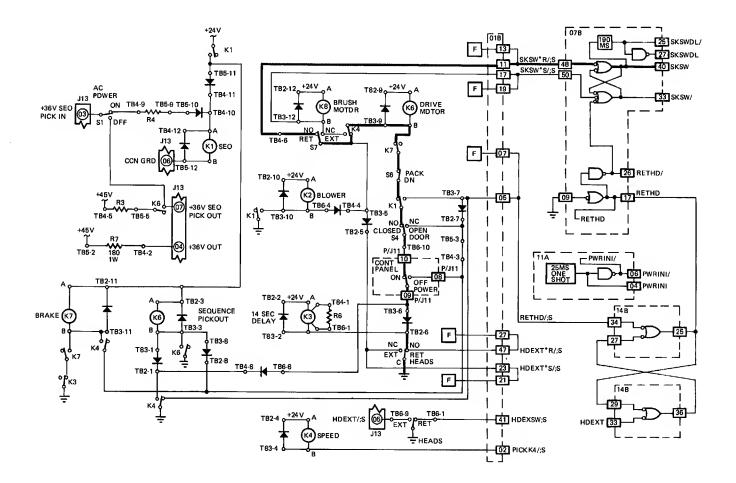
Figure 3-10. Completing Brush Cycle and Initializing First Seek

MOVING CARRIAGE DURING FIRST SEEK

The positioning system causes the carriage to move from the retracted position and the following events occur:

- The head carriage moves forward, closing heads extended microswitches, causing an alternate hold path for K5 and also causing HDEXT*S/;S, HDEXT/;S low and HDEXSW;S high

- HDEXT/;S low provides a heads-extended status signal to the controller and develops a busy status signal (CBSY/) for controller interrogation

- HDEXSW;S high disables the servo hold logic, allowing the carriage to move from the retracted position. If the heads are not extended within 190

milliseconds SKSWDL/ enables the servo hold logic, thereby holding the heads in the retracted position

- HDEXT*S/S low sets the heads extended latch in the status logic and develops access on line to set the ON LINE flip-flop

- When the head carriage detents at cylinder zero, seek ready status signals and ACCOL develop the gated attention signal to the controller, indicating power-up and first seek operations are complete. Figure 3-12 is a flow diagram summarizing the controller initiated power-up sequence
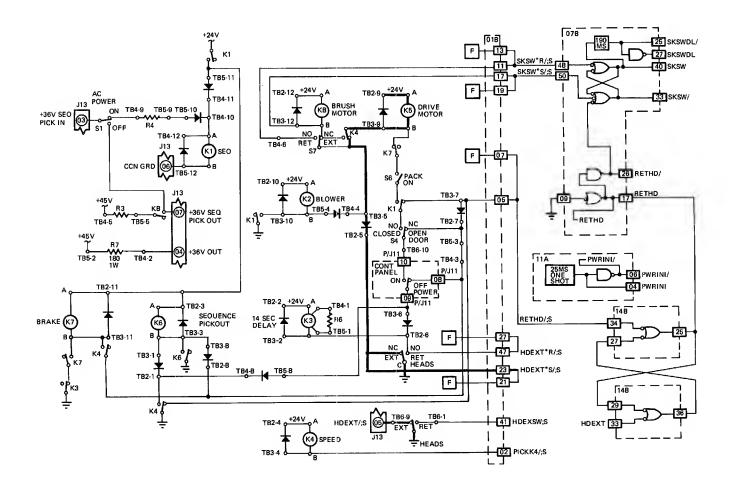
Figure 3-11. Moving Carriage During First Seek
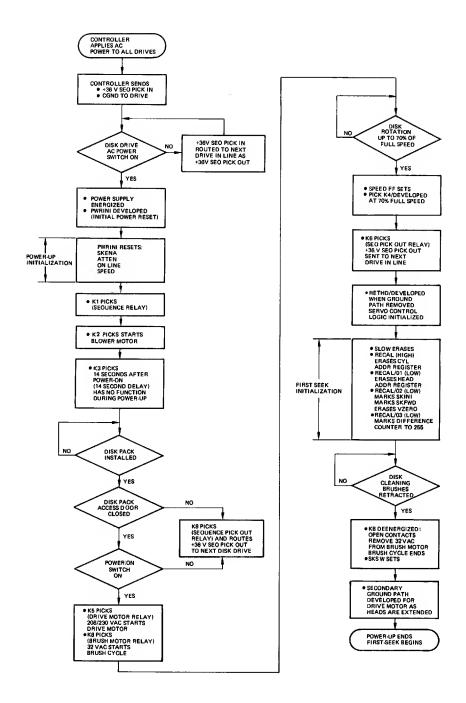
Figure 3-12. Controller Initiated Power-Up, Flow Diagram

STAND ALONE POWER-UP SEQUENCE

If the disk drive is not connected to the controller +36V SEQ PICK IN and CGND are derived internally by jumpering +36 OUT (J3-CL) to +36V SEQ PICK IN (J3-CM) and CGND (J3-CK) to ground (J3-CP). Ac power is derived from site power. After sequence relay K1 energizes, the power-up sequence proceeds with the same qualification as system power-up. Figure 3-13 is a flow diagram summarizing the stand alone power-up sequence.
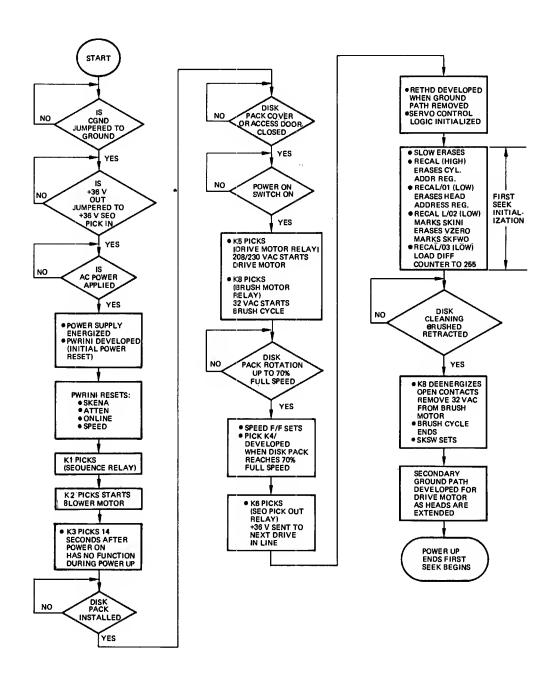
Figure 3-13. Stand Alone Power-Up, Flow Diagram

SECTOR/INDEX AND SPEED DETECTION

The sector/index and speed detection logic (Figure 3-14) comprises an index/sector disk, a transducer, an operational amplifier configured as a threshold detector, logic gates, three one-shots, a flip-flop, and a relay driver.

The task of the index and speed detection logic is to:

- Monitor index pulses developed by the rotating index/sector disk

- Provide index pulses to error detection logic and output status logic
- Determine when disk pack rotation achieves 70 percent of normal operating speed (safe condition to sustain head flight)
- Provide up-to-speed signal to power sequence circuits and error detection logic

The operating disk drive utilizes a standard interchangeable disk pack (Figure 3-15). The bottom disk of the disk pack contains a single index notch machined into the edge.
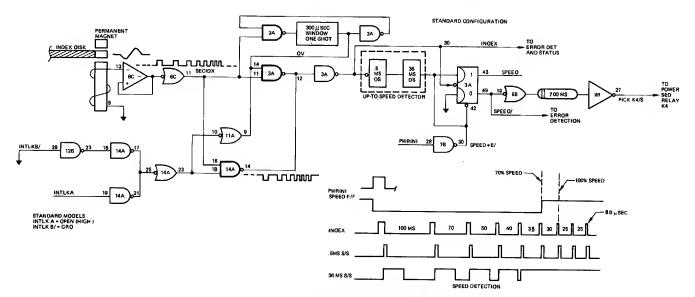
Figure 3-14. Sector/Index and Speed Detection Logic
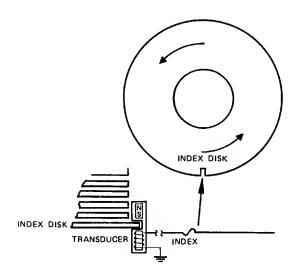
Figure 3-15. Sector/Index Disk and Transducer

Sector/Index Transducer

A magnetic transducer is used in conjunction with the sector/index disk. The transducer is fixed on a hinged assembly, and the hinged assembly is mounted on the deck plate.

When the disk pack is mounted, the transducer is positioned to enclose the edge of the rotating sector/index disk.

As the disk pack rotates, the following occurs:

- The notches in the disk create an air gap during which the magnetic field from the transducer magnet is coupled to the transducer coil
- When the disk interrupts the magnetic field, there is effectively no coupling
- As the disk rotates, the transducer develops pulses during each notch and a pulse train is provided to the sector logic/index and speed detection logic

Speed Detection

The index and speed detection logic operates in conjunction with the index transducer and threshold detector. With each notch sensed, a positive-going index pulse (SECIDX) is produced. As the notched disk rotates, an index pulse train is developed with pulse durations that decrease as the disk pack speed increases. The pulse train is applied to three 2-input NAND gates which are outlined in Figure 3-14.

One of the NAND gates drives a 300-microsecond one-shot which is used to separate the index pulses from the sector pulses disabled for the standard model disk drive by the fact that INTLKA is open (high).

In the standard model drive, INTLKB/ is at ground and INTLKA is open at all times. INTLKA high is applied to an inverter. The low output is inverted twice, then disables the sector/index window logic by clamping the output of the 300-microsecond one-shot to ground and disabling the second NAND gate.

The third NAND gate that is fed by SECIDX has its other input always high because of INTLKA, thus the NAND gates output is a negative going index pulse train. The pulse train is inverted and sent to error detection logic and output status logic. At controller interrogation time, the INDEX pulse train provides 80-microsecond CIDX/ timing pulses to the controller for data transfer synchronization purposes.

The INDEX pulse train is an input to a 36-millisecond holdover circuit comprising a 0.5 millisecond and 36-millisecond one-shot. The 0.5-millisecond one-shot provides a pulse long enough to charge the input capacitor in the 36-millisecond one-shot (see Figure 3-16).

With each negative transition (trailing edge) of the INDEX pulse, the 0.5-millisecond one-shot provides a high output to start the 36-millisecond one-shot. The high output of the 36-millisecond one-shot is applied to the set and erase inputs of the SPEED flip-flop.

As the disk pack starts rotating, the index pulse repetition rate exceeds 36 milliseconds, allowing the 36-millisecond one-shot to turn off. The negative transition from the one-shot is applied to the erase input of the SPEED flip-flop, erasing the flip-flop every revolution.

The 36-millisecond one-shot continues turning on and off until the disk pack reaches approximately 70 percent of rotational speed (1680 revolutions per minute). At this time index pulses are occurring every 36 milliseconds, keeping the 36-millisecond one-shot on. The high one-shot output, is applied to the set input of the SPEED flip-flop and sets the flip-flop when the next INDEX pulse occurs (clock input goes negative). When the SPEED flip-flop sets, the relay driver develops PICK K4/S, after a 700-millisecond delay to energize K4 in the power-up. circuit. When the disk pack reaches full operating speed, (approximately 2400±48 rpm) index pulses occur every 25 milliseconds. The 36-millisecond one-shot remains high, keeping the SPEED flip-flop set.

The read/write heads are retracted from the disk pack if the SPEED flip-flop is erased because of the following conditions:

- If disk pack operating speed is reduced 30 percent, the index repetition-rate exceeds the period of the 36-millisecond one-shot. The one-shot turns off erasing the SPEED flip-flop
- If the disk pack access door is opened, while the disk pack is up to speed, the index transducer is moved away from the rotating disk pack disabling index pulse generation. The 36-millisecond one-shot turns off and erases the SPEED flip-flop
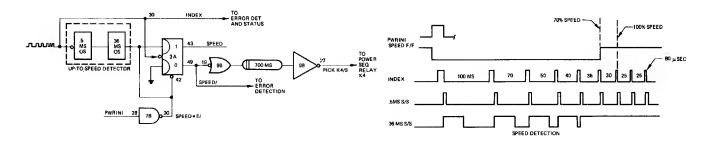
Figure 3-16. Speed Detection

POWER-DOWN SEQUENCE

The main objective of the power-down sequence is to retract the read/write heads from the disk pack and then remove ac power from the disk pack drive motor. The power-down sequence may be initiated in any one of three ways:

- Controller — Initiated

    1. Controlled ground (CGND) removed from all drives, K1 drops causing servo control logic to retract read/write heads

    2. Controller drops ac to all drives when all read/write heads are retracted

- Operator — Initiated

    1. ON/OFF switch set to OFF causes servo control logic to retract read/write heads

    2. The retracted heads remove ac power from disk pack drive motor, and energizes Brake relay K7

    3. Disk pack rotation stops within 12 seconds

- Unscheduled Power Down — An unscheduled event such as ac power failure or disk pack drive motor belt breaking can also cause a power-down sequence to occur.

Figures 3-17 and 3-18 describe the controller-initiated power-down sequence. Figure 3-19 and 3-20 describe the operator-initiated power-down sequence. Figure 3-21 shows the timing for both an operator and a controller initiated power-down sequence.
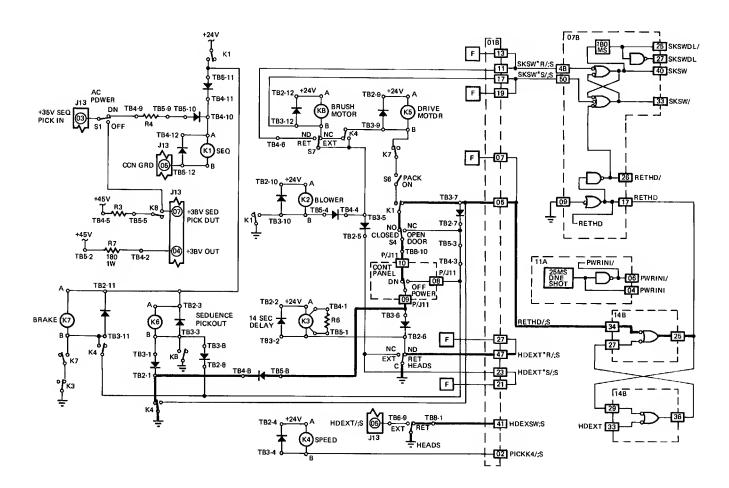
Figure 3-17. Controller-Initiated, Power-Down Sequence

Controller-Initiated Power-Down Sequence

To initiate a power-down sequence the controller removes CGND from all K1 Sequence relays in the system and the following events occur:

- K1 deenergizes opening one of the two ground energizing paths for Drive Motor relay K5
- The energizing path is via the following elements: Ground — through K1 — power on — Drawer Closed — Pack on — K7 contacts — Drive Motor relay
- When K1 deenergizes, ground is routed through K4 and K1 contacts (speed is still up), to the RETHD gates
- RETHD goes high to initiate a retract head operation
- RETHD high erases SKINI and marks SLOW to produce SKFWD*E/
- SKFWD*E/ erases SKFWD flip-flop
- SKFWD/ conditions the REV/ drive gate for subsequent reverse drive
- SKENA sets one clock time after SLOW goes high and enables two control gates:

1. VSLOW/ — Turns on the third least significant D-A converter switch for slow speed drive
2. REV/ — Provides reverse drive direction control and the carriage is driven in reverse at slow speed to the retracted position

As the head carriage moves into the retracted position, head extended switches move to the RETracted position and initiate the following sequence of events:

- HDEXT*R/S resets the heads-extended latch and turns off the device letter (ready) indicator
- HDEXSW;S goes low; activates the servo hold circuits to hold the carriage in the retracted position, and removes current from the drive motor
- When the controller determines HDEXT/ high (heads retracted) from all drives in the system, it drops ac power to all drives

- The remaining relays deenergize
- The drive motor coasts to a stop and the power-down sequence terminates

Figure 3-18 is a flow diagram summarizing the controller-initiated power-down sequence.
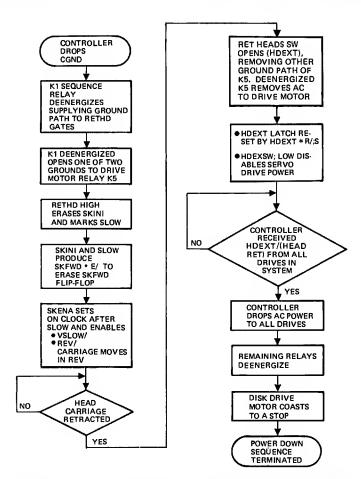
Figure 3-18. Controller-Initiated, Power-Down Sequence, Flow Diagram

OPERATOR-INITIATED, POWER-DOWN SEQUENCE

The sequence of events occurring during an operator-initiated, power-down sequence are similar to the controller-initiated, power-down. The significant differences are:

- The disk pack does not coast to a stop as in controller-initiated, power-down
- A dynamic braking voltage is applied to the disk pack drive motor, stopping disk pack rotation within approximately 12 seconds

When the ON/OFF switch is set to OFF, the following sequence of events occur:

- The ground path is supplied to RETHD gates and the heads are retracted by the same logic used for controller-initiated, power-down
- The ON/OFF switch OFF contacts route ground to energize Brake relay K7 through closed K4 contacts and K1 contacts
- The ON/OFF switch OFF contacts and K7 energized opens one of the ground paths to Drive Motor relay K5

- The head switches move to the retracted position, and the alternate ground path for K5 is broken. A ground path is established to energize 14 second Delay relay K3
- +45 vdc is applied to the drive motor windings, through K7 off contacts, as a dynamic braking voltage (see Figure 3-3)
- When disk pack rotational speed drops 30 percent, K4 deenergizes and removes a ground path to Brake relay K7 through K4 contacts
- A ground path still exists; however, to keep K7 latched through K3 contacts
- Approximately 12 seconds after K7 is energized, K3 energizes opening the remaining ground path to Brake relay K7
- K7 deenergizes, and the dynamic braking voltage is removed, terminating the operator-initiated, power-down sequence

Figure 3-20 is a flow diagram summarizing the operator-initiated, power-down sequence.
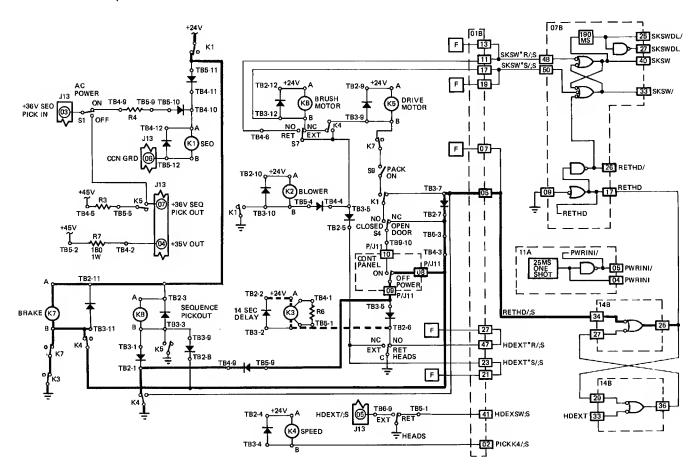
Figure 3-19. Operator-Initiated, Power-Down Sequence

ON/OFF SWITCH
SET TO OFF

OFF CONTACTS OF
ON/OFF SWITCH
• OPEN ONE GROUND
  TO DRIVE MOTOR
  RELAY K5
• ROUTE GROUND TO
  K7 BRAKE RELAY
  THROUGH K4
  CONTACTS

RETHD HIGH
ERASES SKINI
AND MARKS
SLOW TO
PRODUCE
SKFWD * E/ TO
ERASE SKFWD
FLIP-FLOP

SLOW DISABLES
• CYLINDER
  DETECTOR
• DIFF COUNTER
• DAENA GATE

SKENA SETS
ON CLOCK AFTER
SLOW AND
ENABLES
• VSLOW/
• REV/
CARRIAGE MOVES
IN REVERSE

HEAD
CARRIAGE
RETRACTED — NO

YES

• SUPPLY GROUND
  TO 14 SEC
  DELAY RELAY K3
• REMOVE GROUND
  FROM DRIVE
  MOTOR RELAY K5
• APPLY +45VDC
  TO DRIVE MOTOR

DISK
PACK ROTATIONAL
SPEED DROPPED
30% — NO

YES

DEENERGIZE
SPEED RELAY
K4

14
SECONDS
ELAPSED SINCE
DYNAMIC BRAKE
VOLTAGE APPLIED
TO DRIVE
MOTOR — NO

YES

K3 DELAY RELAY
ENERGIZES AND
DEENERGIZES K7
BRAKE RELAY
BY OPENING ONLY
AVAILABLE GROUND
PATH TO K7

DISK PACK
ROTATION HAS
STOPPED
AND DYNAMIC
BRAKE VOLTAGE
IS REMOVED

POWER DOWN
SEQUENCE
TERMINATED

Figure 3-20. Operator-Initiated, Power-Down, Flow Diagram

Unscheduled Power-Down Sequence

If for any reason, the disk pack drive motor speed drops approximately 30 percent, the sector/index detection logic senses the change and deenergizes SPEED relay K4. If the disk pack access door is opened, the index transducer is retracted causing the SPEED flip-flop to be erased and K4 to deenergize.

When SPEED is reset with the heads extended, error detection logic initiates an emergency retract to move the heads to the retracted position. The HDEXT latch resets, and the device letter (ready) indicator turns off, ending the power-down sequence. The loss of input ac power can also cause an unscheduled power-down. Losing input ac power causes a loss of dc supply voltages resulting in the heads being retracted. The emergency retract logic circuits are described later in text. Figure 3-21 is a power-up/power-down timing diagram.
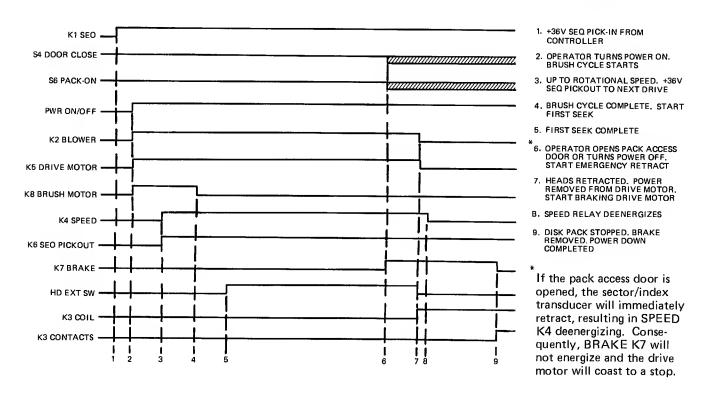
Figure 3-21. Power-Up/Power-Down, Timing Diagram

POSITIONING SYSTEM

The positioning system provides the means of locating the read/write heads at a given cylinder. The positioning system, as shown in Figure 3-22, consists of two major elements: servo system control and servo system.

The servo system control provides logic to direct the servo system in the velocity mode and detent mode. The velocity mode moves the read/write heads to a new cylinder position. The detent mode maintains the heads at a specified cylinder position. The read/write heads are mounted to a head carriage and the head carriage is attached to a linear motor bobbin (Figure 3-23).

The servo system converts a positioning voltage to a linear motor drive current. The interaction of the drive current, linear motor bobbin, and the motor magnet influence moves the linear motor bobbin in either a forward or reverse direction and thus positions the read/write heads.

Figure 3-22. Positioning System, Simplified Block Diagram
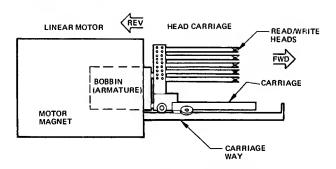
Figure 3-23. Head Carriage and Linear Motor

Feedback is provided to control and limit carriage speed and control the gain of the servo system. The servo system control provides the logic to direct the servo system during first seeks, restore operations, and program seeks. A first seek is performed as a result of a power-up sequence and causes the read/write heads to be positioned at cylinder 000. A restore operation is initiated when the controller issues a restore command or when the physical position of the ID plug is changed. In either case a restore operation causes positioning of the heads to cylinder 000. A program seek operation is performed when the controller commands the read/write heads to a new cylinder position.

The servo system is a closed loop analog circuit that incorporates mechanical, electronic, and electromagnetic components. The system operates either in the velocity mode or the detent mode. In the velocity mode the head carriage is moved from a detent position to the selected cylinder position. In the detent mode the heads are moved into and maintained at the center of the selected cylinder by the null-seeking action of the servo. Figure 3-24 is a block diagram of the servo system. The following is a brief description of the major elements included in the servo system:
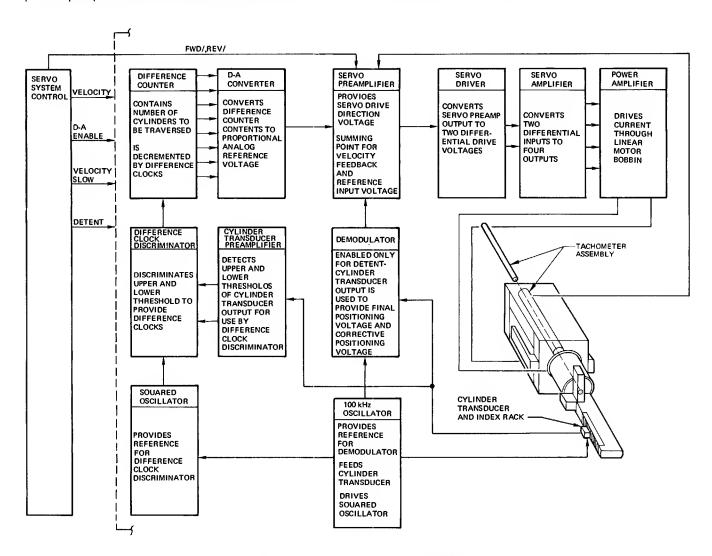
Figure 3-24. Positioning System, Block Diagram

- Index Rack and Cylinder Transducer — provides modulated signal to determine (1) when the head carriage traversed a cylinder position during velocity mode and (2) corrective input to the servo preamplifier during the detent mode
- Cylinder Transducer Preamplifier — converts the cylinder transducer output signal to upper and lower threshold signals for use by the difference clock discriminator
- Difference Clock Discriminator — discriminates upper and lower threshold signals to provide difference clocks to difference counter   .
- Difference Counter — contains number of cylinders to be traversed and is decremented by difference clocks until its contents are equal to zero
- D-A Converter — produces analog voltage from the contents of the difference counter
- Servo Preamplifier — provides direction control to the servo amplifier and sums tachometer negative feedback voltage to attain servo loop stabilization. The output polarity determines the direction of

carriage travel and amplitude determines acceleration.
- Servo Drive Circuits — the servo driver, servo amplifier, and power amplifiers comprise the servo drive circuits. These elements perform a voltage and current amplifying function and provide drive current to the linear motor
- Linear Motor — moves the head carriage to position the read/write heads at the selected cylinder
- Tachometer Assembly — provides servo system feedback to control carriage velocity and detect zero velocity
- Demodulator — converts modulated cylinder transducer output to servo preamplifier positioning voltage during detent mode

SERVO SYSTEM CONTROL

The servo control logic directs the servo system during first seek, restore, and program seek operations. First seek and restore operations are defined as initial seek. Figure 3-25 is a block diagram defining the functional areas of the servo control logic.
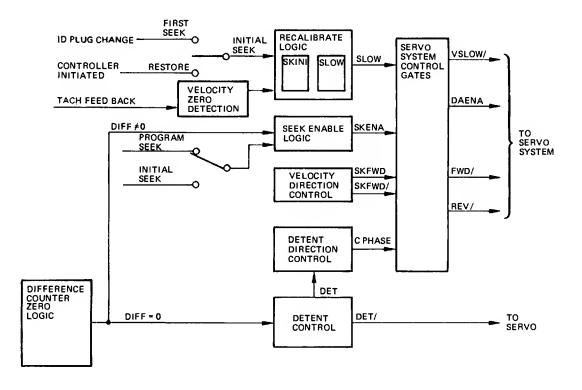
Figure 3-25. Servo Control Logic, Simplified Block Diagram

Figure 3-26 shows the servo system control logic.
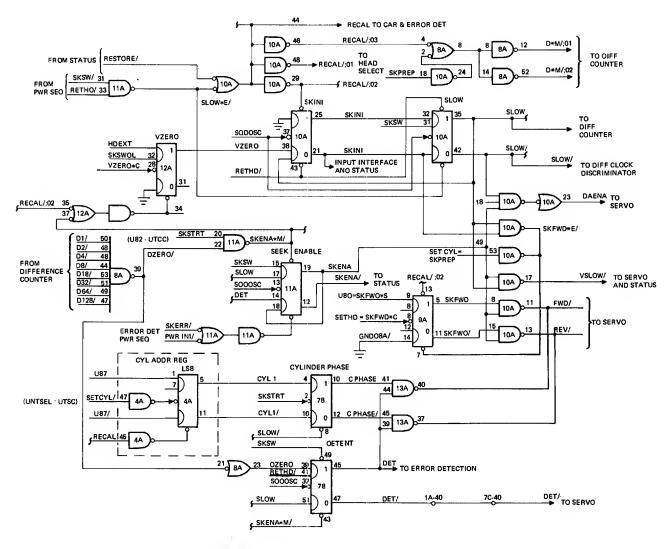
Figure 3-26. Servo System Control, Logic Diagram

To aid in understanding the operating sequences, the basic elements of the logic and their functions are described briefly.

- SKINI (initial seek) and SLOW (slow speed) flip-flops function during first-seek and restore operations. SLOW/ inhibits the difference clock discriminator and thereby disables the difference counter during the forward slow speed drive portion of initial seek. In addition, SLOW conditions the VSLOW/ gate to enable slow servo speed during forward drive

- Recalibrate gates provide RECAL signals that erase the cylinder address register and head address register, mark the difference counter to 255, and

initialize SKINI, SKFWD, SLOW, CPHASE, and VZERO during initial seek operations

- SKENA (seek enable) flip-flop enables the seek logic outputs to the servo system. The state of SKENA controls the D-A enable gate (DAENA), the velocity slow gate (VSLOW/), and the FWD/ and REV/ direction gates

- The state of SKFWD (seek forward), determines the state of FWD/ and REV/. FWD/ and REV/ determine the linear motor drive direction. The state of SKFWD is controlled by initialization logic during initial seek operations and by the controller during program seek operations

- The VZERO (velocity zero) flip-flop sets when the head carriage touches the forward end stop during first seek and restore operations. VZERO set, initiates reverse drive operation
- CPHASE (cylinder phase) flip-flop sets if the least significant bit (LSB) of the cylinder address register is a one (odd) and resets if the LSB is a zero (even). During the detent mode, the state of CPHASE conditions the direction control logic for two reasons:
  1. to provide the final drive direction to position the heads at the desired cylinder
  2. to maintain the heads at the desired cylinder position
- The DETENT flip-flop sets when the difference counter is decremented to zero. When DETENT sets, it resets SKENA which terminates the velocity mode. DETENT set also enables the CPHASE flip-flop gates in the servo control amplifier

First-Seek/Restore (Initial Seek)

The major sequence of events that occur during an initial seek operation are as follows:
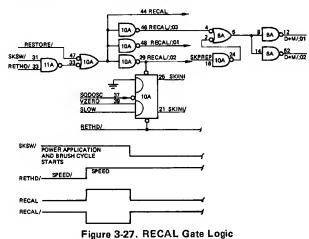
- The difference counter is initially marked to 255
- FWD/ goes low and provides forward direction control for the servo system
- SLOW erases difference counter to 204 by erasing bit positions 32, 16, 2, and 1
- A voltage is enabled from the D-A converter by VSLOW/ low
- The carriage is driven to the end stop at slow speed
- Upon the carriage reaching the end stop, the tachometer detects velocity zero
- REV/ goes low
- The carriage is driven in the reverse direction and the difference counter is decremented as each cylinder position is traversed
- When the difference counter is decremented to zero, the detent flip-flop is set and the heads are maintained at cylinder zero

First-Seek Logical Description — The following paragraphs provide a description of the logical events that occur during a first-seek operation. Included at the end of the description are a flow diagram and timing diagram which summarize the first seek operation. The following conditions are described:

- Initial conditions
- Moving the carriage forward
- Moving the carriage in reverse

During the power-up sequence, when drive motor relay K5 and brush motor relay K8 are energized, the seek switch latch is reset (SKSW/ high) and the disk pack

brush cleaning cycle starts. When the disk pack reaches rotational speed, RETHD/ goes high. RETHD/ and SKSW/ are ANDed to activate the RECAL gates. The RECAL gates are active until the brushes reach their retracted position and set the seek switch latch. Figure 3-27 shows the RECAL gate logic.

Figure 3-27. RECAL Gate Logic

When the RECAL gates are active they perform the following:

- RECAL high is inverted and erases the contents of the cylinder address register and the SKERR flip-flop in the error detection logic
- RECAL/;01 low erases the contents of the head address register
- RECAL/;02 low performs the following:
  1. Marks SKINI and SKFWD flip-flops
  2. Erases VZERO flip-flop
- RECAL/;03 low marks the difference counter to 255

The significant conditions at this time are:

- SKINI and SKFWD are marked and VZERO is erased. Figure 3-28 shows the servo control flip-flops affected by RECAL/;02
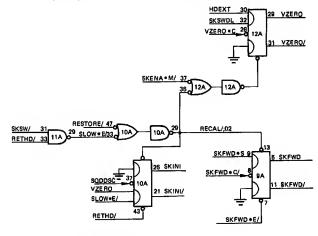
Figure 3-28. RECAL/;02 Logic

3-29

Figure 3-29 shows the logic elements that are used to move the carriage forward.
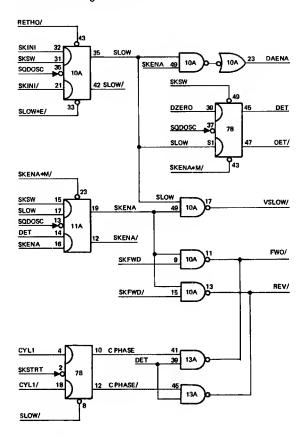
Figure 3-29. Servo Control, Moving Carriage Forward

With SKINI set, SLOW sets on the next clock pulse after SKSW goes high. SLOW being set erases the difference counter to 204. SLOW/ low causes the following:

- Erases the difference clock discriminator flip-flops, preventing decrementing the difference counter while SLOW is active
- Erases the CPHASE flip-flop for detent on an even numbered, cylinder (cylinder zero)
- Disables DAENA to inhibit the difference counter outputs to the D-A converter
- Erases the ONRACK flip-flop

At the next clock pulse, SLOW set and SKSW set cause the SKENA flip-flop to set and the DETENT flip-flop to reset. When the detent flip-flop is reset the CPHASE gates in the servo control amplifier are disabled. Direction control is now provided by the state of the SKFWD flip-flop.

With SKENA set the following occurs:

- VSLOW/ goes low and only the third least significant switch in, the D-A converter is enabled to generate a slow speed drive voltage

- VSLOW/ sets a latch which enables in setting the attention flip-flop at SKRDY time
- FWD/ goes low and provides the forward direction control for the servo system
- A one second seek error time delay is initiated. If detent is not achieved within one second after SKENA is set, the seek error flip-flop in the error detection logic is set.
- SKENA is applied to the set and reset inputs of D1/ in the difference counter but has no effect since SLOW/ has disabled the difference clock circuits

When SKENA sets, the linear motor bobbin begins moving the head carriage in the forward direction at SLOW speed. As the carriage moves out of the retracted position, the heads retracted microswitches transfer to the extended position.

At the beginning of the first-seek operation when the brushes are retracted the seek switch latch (SKSW) sets and triggers the SKSWDLY one-shot. The one-shot goes low for 190 milliseconds. The head carriage must move and activate the heads extended microswitch within the 190 millisecond window, or the servo hold circuits disable the servo system and lock the linear motor bobbin in the retracted position.

The VZERO flip-flop is conditioned by SKSWDLY high which occurs after the 190 millisecond window times out. As the head carriage contacts the end stop, the VZERO flip-flop is set by the negative going edge of the falling tachometer signal (VZERO*C).

With VZERO set, SKINI resets on the next clock pulse. With SKINI/ high and SLOW high, SKFWD*E/ is active, for one SQDOSC clock period, to erase the SKFWD flip-flop. SKFWD low disables the FWD/ motor direction gate and enables the REV/ gate. SKINI/ high causes the SLOW flip-flop to reset on the next clock pulse.

Figure 3-30 shows the logic elements affected during reverse drive.
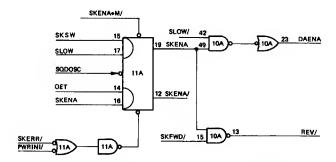
Figure 3-30. Servo Control, Moving Carriage in Reverse

With SLOW reset the following occurs:

- VSLOW/ goes high and disables the slow speed enable to the D-A converter
- The DAENA gate goes high and enables the difference counter outputs to the D-A converter
- The erase inputs to the difference counter and difference clock discriminator are removed

Figure 3-31 and 3-32 are a flow diagram and timing diagram for the first seek operation.

When the DAENA gate enables the difference counter outputs the D-A converter develops the drive voltage that initiates high speed drive and the REV line determines direction. As the head carriage crosses a cylinder position, a cylinder transducer null is detected and the output from the difference clock discriminator (D1*C) decrements the difference counter by one.

When the difference counter is decremented to 201, the ONRACK flip-flop sets with a difference clock (D1*C). This flip-flop and the rack end microswitch are used to detect an off rack condition during a program seek operation.

The process of decrementing the difference counter, as the head carriage traverses a cylinder, continues as the carriage is driven in the reverse direction.

As the head carriage traverses the last cylinder, approaching cylinder zero, the difference counter decrements to zero. DZERO goes high, indicating that the difference counter is zero and on the next clock, the DETENT flip-flop is set. DETENT set enables the CPHASE control gates. (When SLOW/ went low, the CPHASE flip-flop was erased.) CPHASE erased and DETENT set provide the correct direction control to maintain the heads at cylinder zero; that is, when DETENT is set, it enables the demodulator to detect the phase relationship of the cylinder transducer signal.

At the next clock after DETENT set, the SKENA flip-flop resets and terminates the velocity mode.
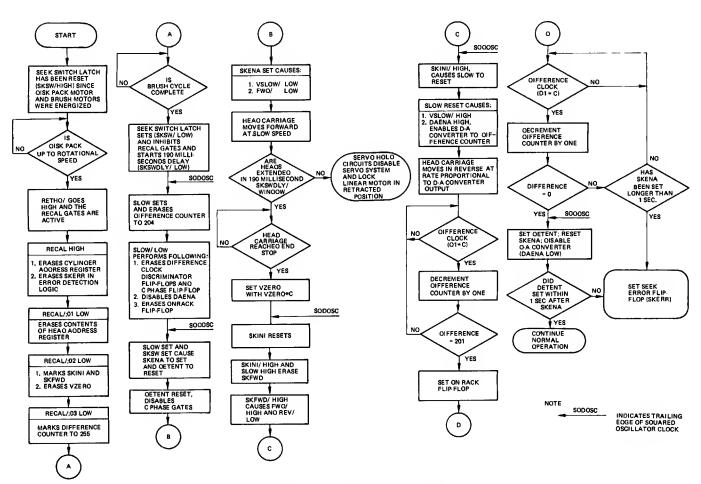
Figure 3-31. First Seek Flow Diagram
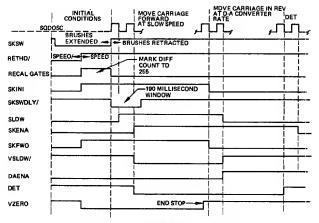
Figure 3-32. First Seek Timing Diagram

While the demodulator is providing reference drive signals to maintain the cylinder zero positioning, the C flip-flop in the difference clock discriminator sets for the last time during the first seek operation. When this occurs a detent time delay begins. The delay is terminated 4 milliseconds later and DETDLY goes high. When DETDLY goes high, SKRDY goes high indicating the drive is ready.

The purpose of detent delay is to wait 4 milliseconds for the read/write heads and servo to settle before sending gated attention back to the controller. The gated attention interrupt is sent to the controller to indicate completion of the seek operation. A CBSY/ signal is available at the interface to indicate that a seek operation has been successfully completed and the disk drive is ready to perform program seek operations.

Restore Logical Description — The restore operation can be initiated by the controller or by changing the ID plug. In either case RESTORE/ goes low and activates the RECAL gates. The remainder of the operation is similar to a first seek. The heads are driven to the end stop from the last cylinder position; not the retracted position as in first seek. The remainder of the operation proceeds with the same qualifications as first seek where ultimately the heads are positioned at cylinder zero. Figures 3-33 and 3-34 are a flow diagram and timing diagram for the restore operation.
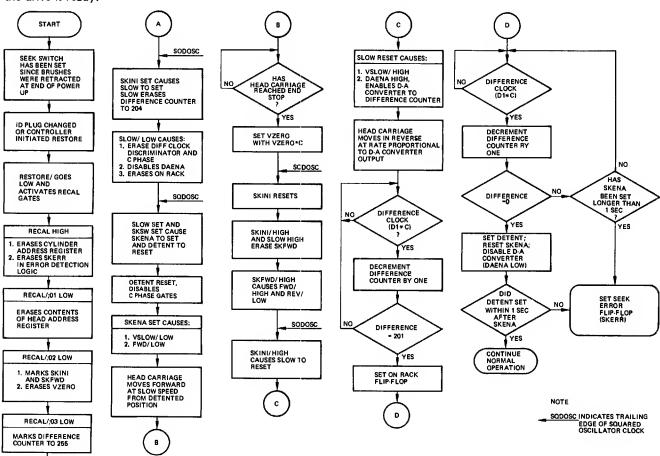
Figure 3-33. Restore Flow Diagram
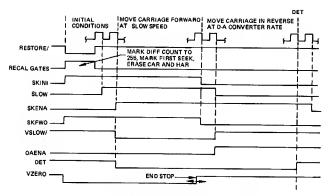
Figure 3-34. Restore Timing Diagram

Program Seek Logical Description

The purpose of program seek is to move the heads from a detent cylinder position to a new cylinder position. Figure 3-35 is a timing diagram of program seek communications between the controller and the disk drive.
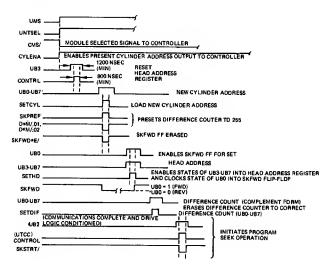
Figure 3-35. Program Seek Communications, Timing Diagram

Figure 3-36 shows the cylinder address register and associated logic.

Prior to moving the heads, the controller selects the disk drive. If the ID switch is in, the present cylinder address is read out to the controller. The controller computes the difference between the present cylinder address and the desired cylinder address. The desired cylinder address is sent from the controller on UB0 — UB7. The states of UB0 — UB7 are clocked into the cylinder address register by SETCYL/.

The following is the sequence of events that occur prior to moving the heads. The numbers separate each set of events.

1. ● Controller selects the disk drive by sending a module select signal (UMS 0—7,S) to the disk drive
   ● Controller reads present cylinder address from cylinder address register
   ● Controller computes the difference between present cylinder address and new address and determines direction in which the carriage should move

2. ● Controller sends UTCC and UB3 back to the disk drive to reset the head address register

3. ● Controller sends the new cylinder address on UB0 — UB7. The states of UB0 — UB7 are clocked into the cylinder address register by SETCYL tag,
   ● SETCYL causes SKPREP
   ● SKPREP develops SKFWD*E/ low which erases the SKFWD flip-flop
   ● SKPREP also develops D*M/;01 and D*M/;02 which presets the difference counter to decimal 255

4. ● Controller transmits the head address on UB3 — UB7 and drive direction bit on UB0
   ● SETHD enables the states of UB3 — UB7 into the head address register and clocks the state of UB0 into the SKFWD flip-flop; UB0 = 0 = REV; UB0 = 1 = FWD

5. ● Controller sends ones complement difference between present and next selected cylinder address on UB0 — UB7. SETDIF enables input gates to again complement UB0 — UB7. The difference is loaded into the difference counter by selectively erasing the corresponding counter flip-flops

6. ● Controller transmits UTCC and UB2 which are ANDed to produce SKSTRT (seek start)
   ● SKSTRT is ANDed with DZERO/ to produce SKENA*M/. SKENA*M/ erases the detent flip-flop and marks SKENA (Figure 3-37).
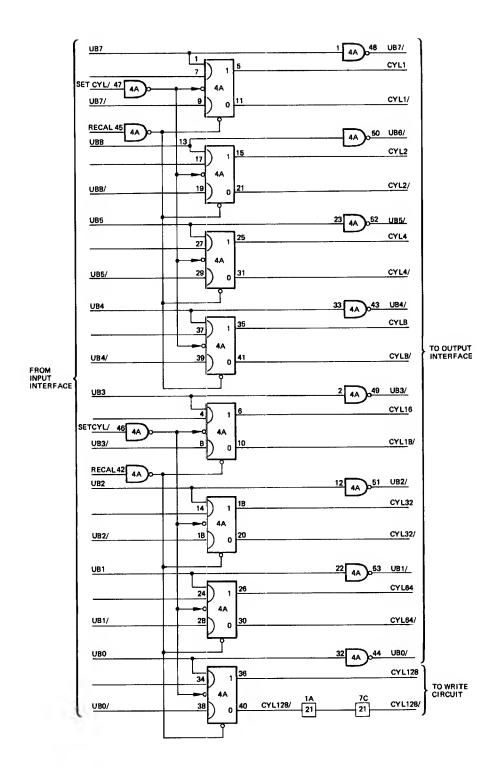
Figure 3-36. Cylinder Address Register Logic
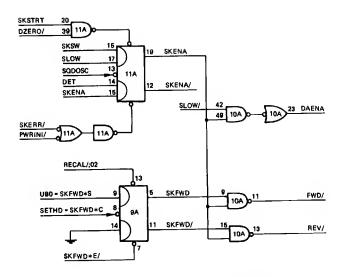
Figure 3-37. Servo Control, D-A Enable and Direction Control

SKENA set causes DAENA to go high and enables either the forward or reverse direction gate depending on the state of SKFWD. When D-A enable goes high the carriage starts moving in the direction as dictated by either FWD/ or REV/. The speed is a function of the value in the difference counter. As the carriage moves, difference clocks (D1*C) are generated which decrement the difference counter by one. Upon the difference counter reaching zero, the DETENT flip-flop is set at the next clock (Figure 3-38). DETENT set enables the demodulator (DET/ low) and enables the state of the CPHASE flip-flop to provide direction control to the servo system during detent.
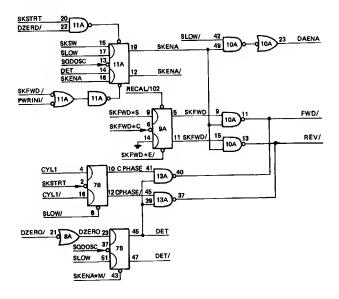
Figure 3-38. Servo Control, Detent

The next clock after DETENT resets SKENA and terminates the velocity mode. While the demodulator is providing reference drive signals to maintain the selected cylinder position, FFC in the difference clock discriminator sets for the last time during the seek operation. When this occurs a detent time delay begins.

The delay is terminated 4 milliseconds later and DETDLY goes high. When DETDLY goes high, SKRDY/ goes low and GTDATN/ goes low. A SKSTAT status signal is dropped by SKRDY and the gated attention signal (CGA0/ — CGA7/) is sent to the controller to indicate completion of the program seek operation. If the drive is still selected, CBSY/ high is sent to the controller to indicate that a program seek operation has been successfully completed and that the drive is ready for the next operation. Figure 3-39 is a timing diagram for the program seek operation. Figure 3-40 is a flow diagram describing the program seek operation.
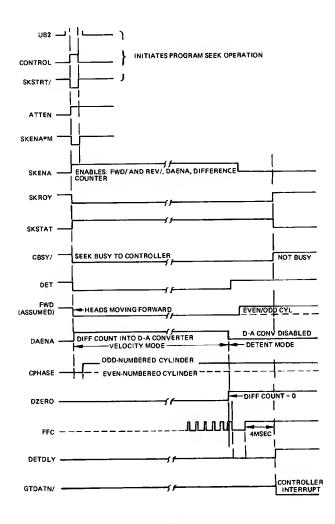
Figure 3-39. Program Seek, Timing Diagram
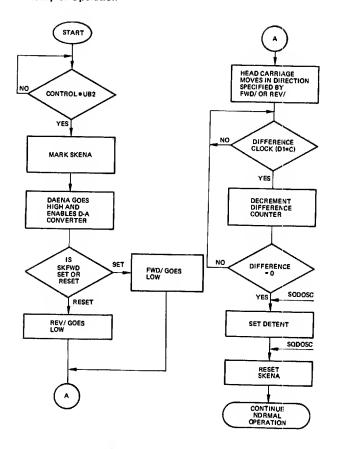
Figure 3-40. Program Seek, Flow Diegram

SERVO SYSTEM FUNCTIONAL DESCRIPTION

The servo system operates in either the velocity mode or detent mode. In the velocity mode, all the major elements are employed except the demodulator. In the detent mode, the demodulator is enabled and the D-A converter is disabled. Included is a functional description of all the servo system major elements and the velocity and detent modes of operation. Figure 3-41 is a detailed block diagram of the servo system.

100 kHz Oscillator and Squared Oscillator

The 100 kHz signal is developed from two transistors and a tank circuit. Figure 3-42 is a simplified schematic of the oscillator circuits.

The 100 kHz oscillator output is supplied through a complementary-symmetry circuit composed of transistors Q4 and Q5. Transistor Q3 provides operating bias and isolates the oscillator from both the output circuits to prevent loading.

The squared oscillator circuit produces two pulses for each cycle of the 100 kHz input signal, or 200,000 pulses per second (200 k pps). Squared oscillator development is shown in Figure 3-43.
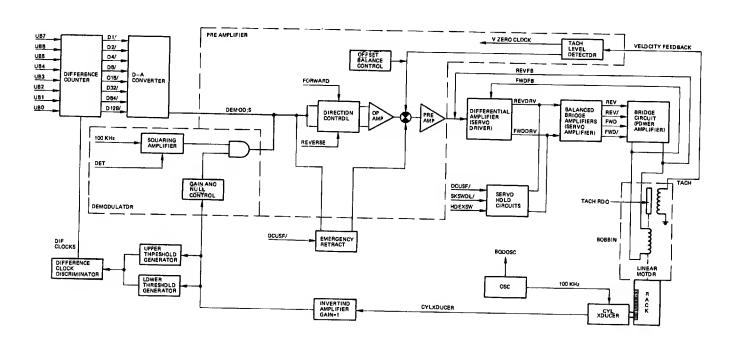
Figure 3-41. Servo System, Detailed Block Diagram
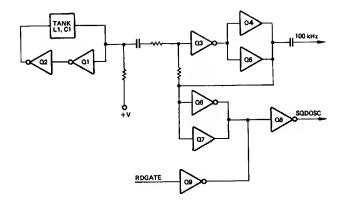
Figure 3-42. 100 kHz Oscillator and Squared Oscillator, Simplified Diagram
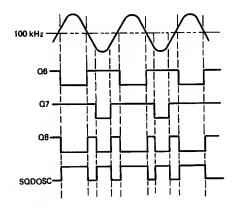
Figure 3-43. Squared Oscillator Development

Transistor Q6 and Q7 are digital switches that perform squaring amplifier functions. Both are biased to remain off until the input signal reaches a given level and then conduct to saturation.

Transistor Q6 (common emitter) is sensitive to positive-going signals only, and transistor Q7 (common base) is sensitive to negative-going signals only. Therefore, Q6 produces a negative pulse for each positive half-cycle of the 100 kHz input and Q7 produces a negative pulse for each negative half-cycle. The common output of the parallel transistors provides a negative-going pulse for each half-cycle of the input signal or two pulses for each cycle of the input signal.

Transistor Q8 amplifies and inverts the double frequency pulse train from transistor Q6 and Q7 and provides the 200 k pps SQDOSC. During read operations, the SQDOSC output is inhibited by RDGATE to minimize noise.

Index Rack and Cylinder Transducer

The index rack and cylinder transducer modulate a 100 kHz reference signal. As the carriage traverses cylinders, the output from the cylinder transducer will be in phase with the 100 kHz reference for one cylinder and out of phase for the next cylinder; except when coming on or leaving the rack.

In addition, the amplitude of the cylinder transducer signal will be at a maximum between cylinders and at a minimum at the center of a cylinder. Thus, as the carriage moves the index rack past the cylinder transducer, the output of the cylinder transducer is a phase- and amplitude-modulated signal. It is the phasing of this signal that provides a means of determining precisely where the head carriage is positioned with respect to a given cylinder location. The amplitude provides a means of detecting cylinder traversals. Figure 3-44 shows the cylinder transducer output.
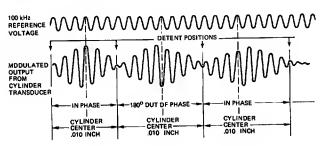
Figure 3-44. Cylinder Transducer/Cylinder Relationship

The nulls provide the means of detecting when the carriage crossed the center of a cylinder and the peaks provide a means of detecting cylinder boundaries.

Cylinder Transducer Preamplifier

The purpose of the cylinder transducer preamp is to detect the 150-millivolt and 200-millivolt cylinder transducer output levels and develop two signals which are used to control the state of three flip-flops in a difference clock discriminator.

The modulated output from the cylinder transducer is fed to two operational amplifiers configured as threshold detectors. When the amplitude of the modulated signal reaches threshold level (150 mv), one of the amplifiers turns on. As the amplitude of the modulated signal increases to the threshold level of the other amplifier (200 mv), it also will turn on. When each amplifier is on, it outputs 100 kHz pulses which are inverted and fed to holdover one-shot circuits. As the first 100 kHz pulse is fed into a one-shot, the one-shot output goes high. As long as the 100 kHz pulses are present, the output of the one-shot remains high because the period of the one-shot is greater than the period of the 100 kHz (10

microseconds). Conversely, the output of the one-shots will drop low when the cylinder transducer amplitude falls below the threshold level of the amplifiers. The two outputs from the cylinder transducer preamplifiers are defined as upper threshold and lower threshold and are used to control the states of the difference clock discriminator. Figure 3-45 is a block diagram of the cylinder transducer preamplifier.
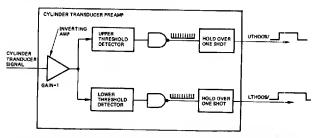
Figure 3-45. Cylinder Transducer Preamplifier, Block Diagram

Difference Clock Discriminator

The purpose of the difference clock discriminator is to generate one difference clock per cylinder crossed from the states of the upper and lower threshold signals. The upper and lower thresholds control the states of three flip-flops in the difference clock discriminator. When the states of the three flip-flops are in a given condition, two of their outputs are ANDed with the SQDOSC and the resultant signal is the difference clock. The difference clock is then used to decrement the difference counter. A difference clock is generated each time the read/write heads traverse a cylinder position. Figure 3-46 shows the difference clock discriminator and cylinder transducer. Figure 3-47 shows the difference clock discriminator timing.
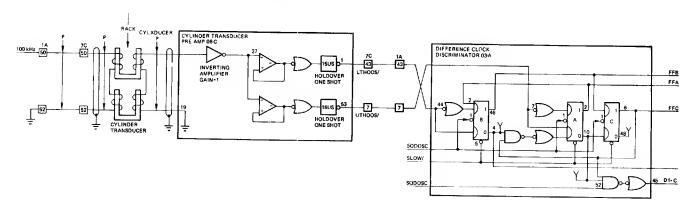
Figure 3-46. Cylinder Transducer Preamp and Difference Clock Discriminator
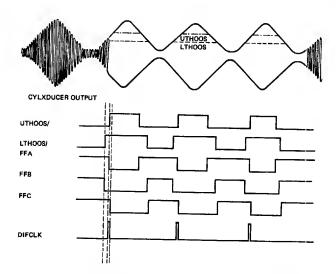
Figure 3-47. Difference Clock Discriminator, Timing Diagram

Difference Counter

The difference counter is an eight bit register loaded from the controller during program seeks or preset by the servo control logic during first seeks and restore operations. The value loaded in the difference counter during program seeks is the difference between the present cylinder address and the desired cylinder address. As the carriage moves past each cylinder position a difference clock is generated which decrements the difference count by one. When the difference counter is equal to zero, the detent mode is initiated by the servo control logic. Figure 3-48 shows the difference counter logic.
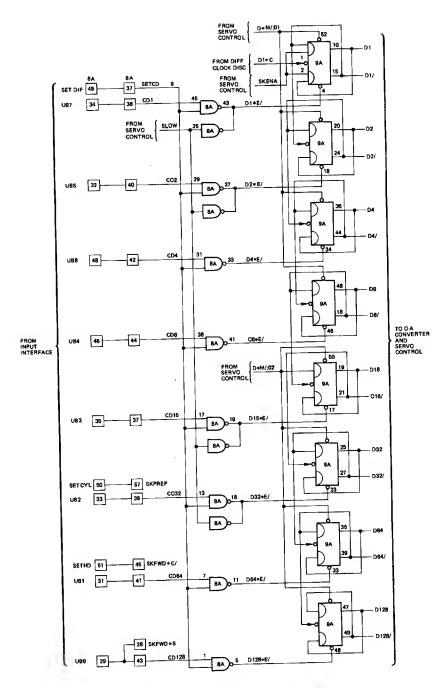
Figure 3-48. Difference Counter, Logic Diagram

At the beginning of any seek operation all bit positions are marked to 255 by D*M/;01 and D*M/;02. During initial seek (first seek or restore) preset gates activated by SLOW erase bit positions D1, D2, D16, and D32 causing the difference to be 204. During program seek, when SETDIF is high, the states of UB0 – UB7

selectively erase the counter from 255 to the specified difference value.

The counter is decremented by each D1*C (difference clock) because the reset side of each bit is connected as the clock input to the next higher bit, except for D1. The clock input to D1 is D1*C.

D-A Converter

The D-A converter is a seven step ladder-adder which produces an analog voltage proportional to the digital contents of the difference counter. The D-A converter provides a reference voltage to the servo control amplifier. The servo preamplifier and the associated servo amplifier/driver elements provide a drive current to drive the linear motor. Figure 3-49 shows the D-A converter.
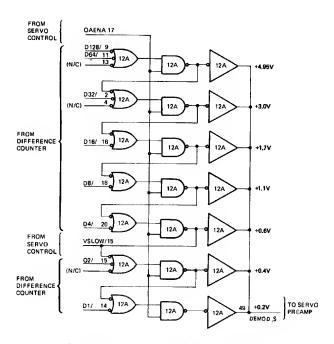
Figure 3-49. D-A Converter, Logic Diagram

When the D-A converter is enabled (DAENA), an analog voltage is generated that is directly proportional to the highest order bit stored in the difference counter. The operation is such that the adder switches are turned off starting with the most-significant bit (MSB). As the difference counter is decremented, the logical low of each next most significant input causes the switches associated with that digit and all lower-order digits to be turned on simultaneously when the decoding gates are enabled. The data inputs change as the difference counter is decremented but the converter is insensitive to all changes except a change affecting the most-significant active digit of the number involved. For example, if D32/ is the most-significant active digit, all switches associated with lower-order digits are turned on simultaneously. As the difference counter is decremented, the switch associated with D32/ is turned off first, then the switch associated with D16/ is turned off, then D8/, etc.

Figure 3-50 shows a typical D-A converter output and the corresponding velocity profile. Note that velocity is highest when the difference is greater than 63 and becomes successively lower as the head carriage approaches the selected cylinder.
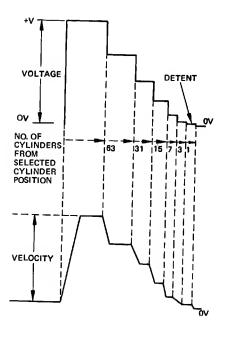
Figure 3-50. D-A Voltage and Velocity Profiles

Tachometer Assembly

The tachometer assembly (Figure 3-51) consists of a magnetic rod inserted within a pickup coil. One end of the magnetic rod is attached to the carriage.
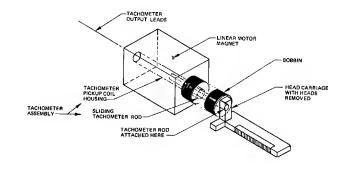
Figure 3-51. Tachometer Assembly

The pickup coil is mounted inside the linear motor. The tachometer functions as a velocity detector and provides feedback to the servo system to control carriage velocity. When the carriage moves in either direction, the moving tachometer rod generates a voltage, in the coil, proportional to the carriage speed. The voltage polarity is determined by the direction of motion: positive voltage is developed during forward motion and negative voltage is developed during reverse motion. The output of the pickup coil is applied to the servo preamplifier where it is amplified and applied as degenerative feedback to the servo driver.

Servo Preamplifier

The servo preamplifier provides a forward or reverse drive voltage during velocity and detent modes. During the velocity mode, the servo preamplifier sums the D-A converter output with the velocity feedback voltage from the tachometer. The FWD/ and REV/ signals from the servo control logic determine the polarity of the output and thus control the carriage direction. During the detent mode FWD/, REV/ and CYLINDER;S control the carriage direction. Figure 3-52 is a block diagram of the servo preamplifier, demodulator and emergency retract logic.
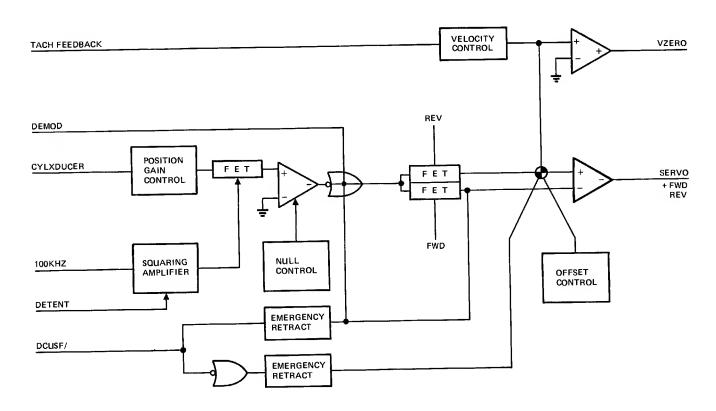
Figure 3-52. Servo System Input Control, Block Diagram

An additional input to the servo preamplifier is from the emergency retract logic. The emergency retract section provides the servo voltages necessary to return the carriage fully when a DC unsafe condition is detected. When an emergency retract condition exists DCUSF/ goes low causing the output of the servo preamplifier to go to -12 volts. This results in the head carriage being retracted.

Servo Driver

The purpose of the servo driver is to convert the voltage input from the servo preamplifier and the forward and reverse feedback from the power amplifier into two differential driving voltages for the servo amplifier. Figure 3-53 is a block diagram of the servo driver.
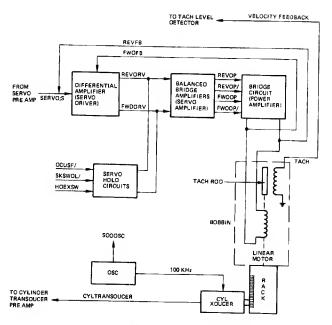
Figure 3-53. Servo Driver, Block Diagram

The servo driver converts the voltage input from the servo preamplifier (SERVO;S); into a differential driving signal. The voltage developed across the linear motor coil serves as a feedback voltage.

A positive SERVO;S input results in a more-positive output (greater than 22 volts) on the forward drive line (FWDDRV) and a less-positive output (less than 22 volts) on the reverse drive line (REVDRV). A negative input results in a less-positive output (less than 22 volts) on the forward drive line and a more-positive output (greater than 22 volts) on the reverse drive line.

A servo hold circuit is activated any time the heads are not extended. However, seek switch delay (SKSWDL/) disables the servo hold circuits for a 190 milliseconds to allow the linear motor to move the head carriage far enough to transfer the heads extended switches.

When the servo hold circuit is active, FWDDRV;S and REVDRV;S are both held at ground. This results in ground being applied to both ends of the linear motor coil.

Servo Amplifier and Power Amplifier

The servo amplifier is essentially a current amplifier that feeds the differential servo-driving signal into the power amplifier circuit. The amplifier consists of two identical differential amplifier circuits, each of which comprises four transistors. Figure 3-54 is a simplified schematic of the servo amplifier and power amplifier.

The current path for the linear motor is determined by one pair of transistors from each differential circuit in the servo amplifier. Transistors Q1, Q3, Q6, and Q8
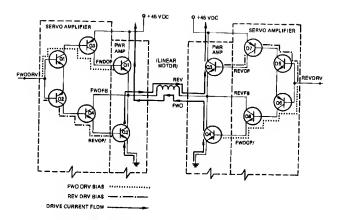
Figure 3-54. Servo Amplifier and Power Amplifier, Simplified Schematic Diagram

work in conjunction to provide bias for forward motor drive; Q2, Q4, Q5, and Q7 provide bias for reverse motor drive. A high input (greater than +22 V) applied to either circuit turns two transistors on and turns two transistors off. If the input is low (less than +22 V), the condition is reversed.

The power amplifier circuit is a bridge circuit which provides a means for switching the direction of current through the linear motor coil. The servo amplifier turns on one pair of power amplifier transistors at a time. As one servo amplifier circuit turns on one pair, the other circuit turns off the other pair; each time the pairs are switched, the direction of current flowing in the coil changes. When power amplifier Q1 and Q4 are ON, the motor drives in the forward direction.When Q2 and Q3 are on the motor drives in the reverse direction.

The following paragraphs describe the operation of the servo system in the velocity mode and detent mode as directed by the servo control logic.

Velocity Mode

The operation of the servo system in the velocity mode has to be considered for first seek and restore (initial seek) and program seek. Figure 3-55 provides a logic diagram of the servo system.

Initial Seek (First Seek or Restore)

Initial conditions from servo control logic during initial seek:

- The difference counter has been marked to 255 and erased to 204
- DAENA is low
- VSLOW/ is low
- DET/ is high
- FWD/ is low
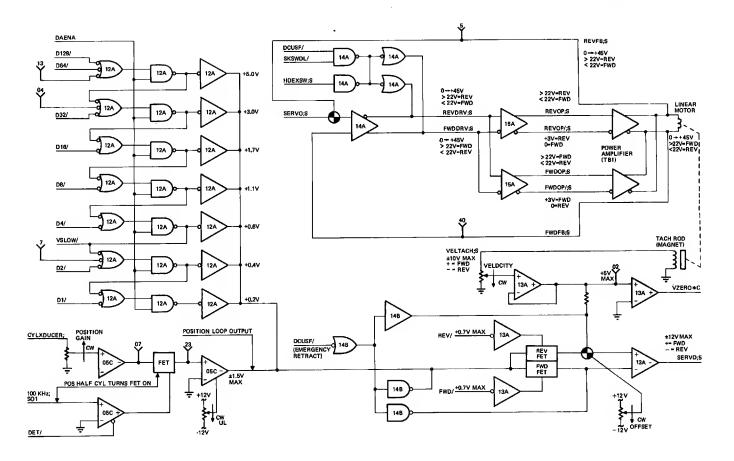
Figure 3-55. Servo System, Logic Diagram

DAENA low inhibits the difference counter inputs to the D-A converter. DET low disables the demodulator section of the servo control amplifier. VSLOW/ low, enables a slow velocity voltage (approximately +0.4V) from the D-A converter to the servo preamplifier. FWD/ low, enables the logic which allows slow velocity voltage to be applied to the inverting input of the servo control operational amplifier. The servo preamplifier then outputs a high positive voltage (SERVO;S) which causes the remainder of the servo drive circuits to develop forward drive. Forward drive current is directed through the linear motor bobbin and the head carriage moves forward at slow speed.

The tachometer then feeds back a positive voltage to the tachometer amplifier in the servo preamplifier decreasing the output at SERVO;S because the output of this amplifier is applied to the summing point. When the carriage reaches the end stop, the tachometer feedback falls and the inverter outputs a velocity zero clock

(VZERO*C) to the servo system control logic. The following then occurs:

- FWD/ goes high
- REV/ goes low
- DAENA goes high

DAENA high enables the output of the difference counter to be converted to a driving voltage by the D-A converter. REV/ low routes the driving voltage to the non-inverting side of the operational amplifier. The amplifier outputs a negative voltage which is converted to a reverse drive by the remainder of the servo circuits and the carriage is driven in the reverse direction. Difference clocks are generated as the carriage traverses each cylinder position and the difference counter is decremented. When the difference counter equals zero DAENA goes low to disable the D-A converter, DET goes high to enable the CPHASE gates in the servo preamplifier, and the detent mode is entered. Figure 3-56 shows when the detent mode is entered.
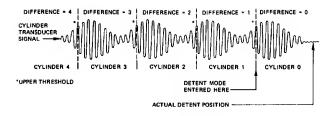
Figure 3-56. Entering Detent Mode

Program Seek

Initial Conditions:

- Controller has loaded difference counter with number of cylinders to be traversed

- Controller has sent direction control bit and either FWD/ or REV/ is active

- Controller sends SKSTRT which marks SKENA, causing DAENA to go high

When DAENA goes high the D-A converter converts the difference counter contents to a proportional analog voltage. The analog voltage is applied to the REV and the FWD FET's of the preamplifier. One of the FET's is enabled by FWD/ or REV/ and passes the analog voltage to the non-inverting or inverting input of the operational amplifier. The carriage is then driven in the appropriate direction at a rate proportional to the sum of the decreasing D-A converter voltage and the tachometer feedback voltage. When the difference counter is decremented to zero, DAENA goes low, DET/ goes low and the detent mode is entered. Figure 3-57 shows the tachometer and D-A converter voltages during a 15 cylinder seek.
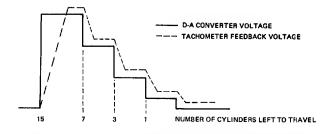
Figure 3-57. D-A Converter and Tachometer Voltage Comparisons During a Fifteen Cylinder Seek

When the D-A converter voltage drops, the tachometer feedback also falls, reflecting the decrease in velocity, but head carriage momentum prevents the linear motor from responding instantaneously to the decreasing drive current and the tachometer feedback voltage remains slightly greater than the D-A converter voltage.

Detent Mode

Initial conditions during detent:

- The difference counter has been decremented to zero

- DET/ is low

- DAENA is low inhibiting the D-A converter

- The state of the CPHASE flip-flop, in the servo system control, indicates whether the selected cylinder's least significant bit (LSB) is even or odd (set=odd, reset=even)

- FWD/ or REV/ is low

When the difference counter decrements to zero, DET/ goes low as the last cylinder to be traversed is crossed and the head carriage approaches the desired cylinder. DET/ low enables the demodulator which outputs a small final drive voltage, sufficient to drive the carriage to the selected cylinder position. The polarity of the voltage is determined by the phase relationship of the cylinder transducer output to the 100 kHz oscillator. This is a function of the last cylinder being crossed (odd or even) and the direction of carriage travel. The state of the least significant cylinder address bit controls the REV and FWD signals which, in turn, determines whether the demodulator output is applied to the inverting or non-inverting input of the operational amplifier.

The servo preamplifier then outputs the necessary voltage to drive the carriage to its final position. Once the heads are in their final position, any carriage movement is sensed by the demodulator and a corrective voltage is supplied to the servo preamplifier. The cylinder address least significant bit continues to control which input of the operational amplifier is being used and thus the output of the servo preamplifier provides a corrective voltage to maintain the heads within microinches of the selected cylinder.

To describe the operation of the demodulator, the operation of the cylinder transducer and index rack have to be considered. The amplitude of the cylinder transducer signal changes as the relative position of the index rack and cylinder transducer changes. When the heads are positioned at a cylinder, the cylinder transducer signal is at a null; the signal reaches maximum amplitude when the heads are between cylinders. With each cylinder traversed, the phase and amplitude of the signal changes in relation to the 100 kHz reference voltage feeding the cylinder transducer. Figure 3-58 shows the cylinder transducer signal. Note only a few cycles of the 100 kHz are shown for simplicity of explanation; bear in mind there are many more cycles per cylinder traversal than shown.
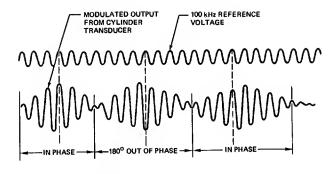
Figure 3-58. Cylinder Transducer Composite Signal

The index rack contains precisely machined teeth. The distance between teeth and the number of teeth provide a cylinder relationship reference. The cylinder transducer is essentially a transformer with two primary coils and two secondary coils. The primary coils are wound in phase with each other (series aiding) and are connected in series to the 100 kHz reference. The secondary coils are wound out of phase with each other (series opposing) and are also connected in series. This arrangement provides one secondary and primary coil that are wound in phase with each other and are in phase with the 100 kHz reference. The other primary and secondary coils are out of phase with each other, and the secondary is out of phase with the 100 kHz reference. Figure 3-59 is a schematic diagram showing this arrangement.
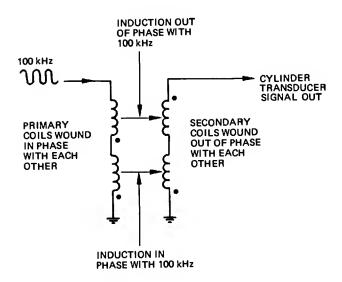
Figure 3-59. Cylinder Transducer, Schematic Diagram

Figure 3-60 shows the actual index rack and cylinder transducer relationship.
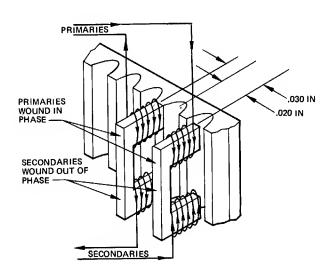
Figure 3-60. Index Rack and Cylinder Transducer Relationship

The index rack valleys are machined on approximately .020-inch centers. The distance between cylinder transducer pole piece centers is approximately .030-inch. The relationship is such, that when one pole piece is positioned directly over a tooth; the other pole piece is over a valley. The pole piece positioned over a tooth obtains maximum primary to secondary coupling; while the pole piece over the valley obtains minimum primary to secondary coupling.

When both pole pieces are positioned equally close to a tooth there will be an equal amount of coupling from each primary to each secondary.

For the purpose of explanation, consider three conditions that exist as the index rack moves past the cylinder transducer.

- If the out-of-phase winding is over a tooth, out-of-phase coupling is maximum. The resultant output will be at maximum amplitude and 180 degrees out of phase with the 100 kHz reference
- If the in-phase windings are over a tooth, in-phase coupling is maximum. The resultant output will be at maximum amplitude and in phase with the 100 kHz reference
- If the in-phase windings and the out-of-phase windings are equally close to a tooth, in-phase coupling and out-of-phase coupling are equal and the resultant output will be minimum (null). Figure 3-61 through 3-63 illustrate the three conditions
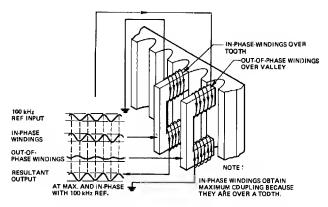
Figure 3-61. In-Phase Windings Over a Tooth
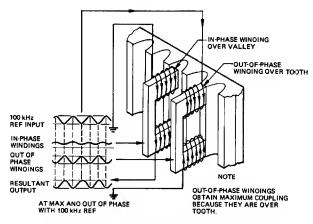
Figure 3-62. Out-of-Phase Windings Over a Tooth
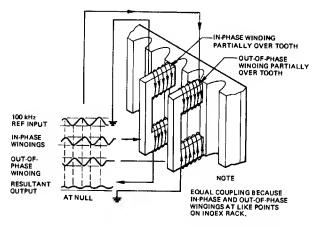
Figure 3-63. In-Phase and Out-of-Phase Windings at Like Points

The three conditions illustrated considered only finite points in time. As the index rack moves past the cylinder transducer, the teeth provide varying degrees of coupling. The actual cylinder transducer output is the algebraic sum of the voltage induced in each opposing secondary.

The output of the transducer is in phase with the 100 kHz for one excursion and 180 degrees out-of-phase for the next excursion. Figure 3-64 shows this relationship.
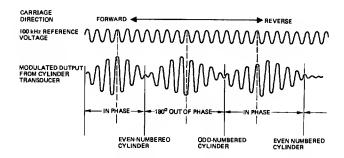
Figure 3-64. Cylinder Transducer/100 kHz Phase Relationship

The demodulator section of the preamplifier uses the 100 kHz oscillator pulses to convert the cylinder transducer signal to a fine positioning voltage for the servo preamplifier section. The 100 kHz signal enters an amplifier and squaring circuit that feeds a gating circuit (Figure 3-65). The amplifier is enabled during detent and
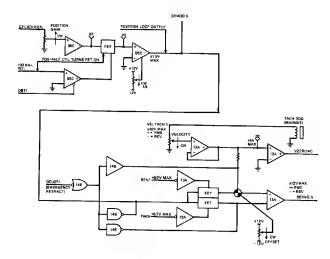
Figure 3-65. Demodulator, Logic Diagram

the FET gate passes CYLXDUCER signal that occur during the positive half-cycle of the 100 kHz.

During detent the cylinder transducer output becomes a series of pulses either above or below ground as determined by crossing from an odd to an even cylinder or vice versa. Thus, the cylinder transducer signal present during the oscillator positive half-cycle is sent to the servo operational amplifier.

The servo operational amplifier thus converts the pulses, which may be of either polarity, to a dc voltage whose amplitude is a function of the distance that the carriage is from the desired cylinder. The polarity of the signal represents the direction that the head carriage should move.

Figure 3-66 shows the cylinder transducer and demodulator output relationship.

*NOTE:
THESE SIGNALS DO NOT ACTUALLY OCCUR UNTIL DETENT IS SET. THEY ARE SHOWN FOR EXPLANATION OF CIRCUIT ONLY.
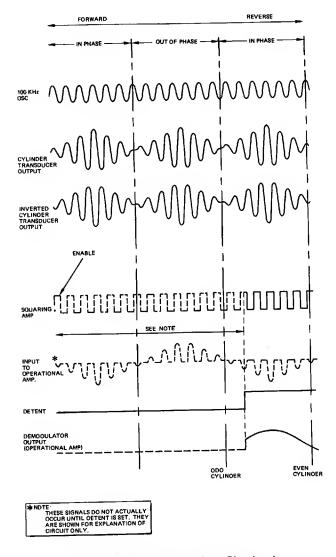
Figure 3-66. Cylinder Transducer Signal and Demodulator Output Relationship

The demodulator output, DEMOD;S, is subsequently applied to FWD and REV FET gates of the preamplifier as a low amplitude positive or negative voltage. The state

of CPHASE flip-flop determines which FET gate active, allowing the DEMOD's signal to be applied to either the inverting or non-inverting input of the operational amplifier.

The CPHASE flip-flop is set by the least significant cylinder address bit and controls the operational amplifier input. As a result, the phase relationship of the final cylinder crossing is known and consequently the polarity of the pulses presented to the operational amplifier is known; thus the proper input (inverting or non-inverting to the operational amplifier is selected.

From Figure 3-66 it can be seen that there is a specific relationship between the following:

- Carriage direction

- Phase relationship of 100 kHz and cylinder transducer signals

- Whether next cylinder is odd or even

- Demodulator polarity

The phase relationship is as follows:

CARRIAGE DIRECTION	NEXT CYL.	PHASE REF	DEMOD POLARITY	SERVO CONTROL AMP OUTPUT
FWD	ODD	IN PHASE	+	+
FWD	EVEN	180°OUT	-	+
REV	EVEN	IN PHASE	+	-
REV	ODD	180°OUT	-	-

The output from the demodulator is then applied to the input of the servo preamplifier section. CPHASE is set if the least significant bit of the cylinder address is a one and is reset if the least significant bit is a zero. If CPHASE is set, it directs the cylinder transducer signal to the non-inverting input of the operational amplifier. If CPHASE is reset it directs the cylinder transducer output to the inverting input of the operational amplifier.

Since there is a relationship between the carriage direction and selected cylinder four conditions exist. Figure 3-67 through Figure 3-70 describe the four conditions.

Forward to Odd Cylinder —

- Direction is forward

- The cylinder pulses are in phase with the 100 kHz signal

- The FET output of the demodulator is a series of negative going pulses whose amplitude is proportional to the CYLXDUCER pulses. Thus, the output of the demodulator is a positive voltage.

- CPHASE is set, enabling the FWD FET of the servo preamplifier

- The positive going demodulator output signal is applied through the FWD FET to the

non-inverting input of the servo preamplifier whose positive output provides more forward drive

- The carriage then moves into a null or zero volt position

- As the carriage passes the null the demodulator output swings negative

- The negative voltage, applied through the FWD FET to the non-inverting input of the operational amplifier, produces reverse drive voltage to stop carriage at the desired cylinder

- The positioning systems maintains this balance during detent
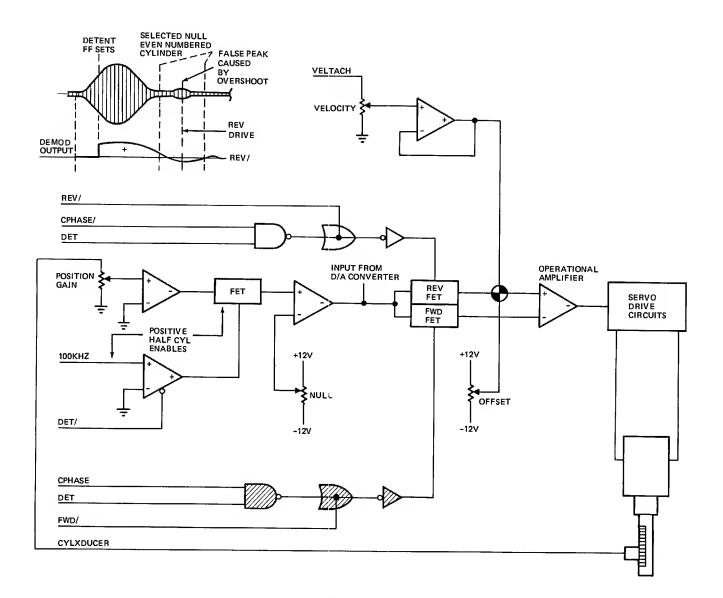
Figure 3-67. Detent Condition 1, Forward to Odd Cylinder

Forward to Even Cylinder —

- Direction is forward

- The cylinder pulses are out of phase with the 100 kHz signal

- The FET output of the demodulator is a series of positive going pulses whose amplitude is proportional to the CYLXDUCER pulses. Thus, the output of the demodulator is a negative voltage

- CPHASE is reset, enabling the REV FET of the servo preamplifier

- The negative demodulator output signal is applied through the REV FET to the inverting input of

the servo preamplifier whose positive output provides more forward drive.

- The carriage then moves into a null or zero volt position

- As the carriage passes the null the demodulator output swings positive

- The positive voltage, applied through the REV FET to the inverting input of the operational amplifier, produces reverse drive voltage to stop the carriage at the desired cylinder

- The positioning systems maintains this balance during detent
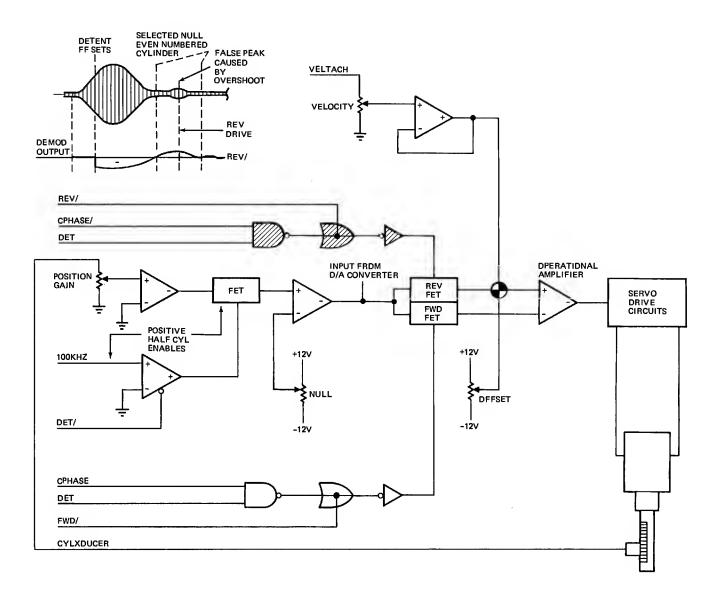
Figure 3-68. Detent Condition 2, Forward to Even Cylinder

Reverse to Even Cylinder —

- Direction is reverse

- The cylinder pulses are in phase with the 100 kHz signal

- The FET output of the demodulator is a series of negative going pulses whose amplitude is proportional to the CYLXDUCER pulses. Thus, the output of the demodulator is a positive voltage

- CPHASE is reset, enabling the REV FET of the servo preamplifier

- The positive going demodulator output signal is applied through the REV FET to the inverting

input of the servo preamplifier whose negative output provides more reverse drive.

- The carriage then moves into a null or zero volt position

- As the carriage passes the null the demodulator output swings negative

- The negative voltage, applied through the REV FET to the inverting input of the operational amplifier, produces forward drive voltage to stop the carriage at the desired cylinder

- The positioning systems maintains this balance during detent

Figure 3-69. Detent Condition 3, Reverse to Even Cylinder

Reverse to Odd Cylinder —

- Direction is reverse

- The cylinder pulses are out of phase with the 100 kHz signal

- The FET output of the demodulator is a series of positive going pulses whose amplitude is proportional to the CYLXDUCER pulses. Thus, the output of the demodulator is a negative voltage

- CPHASE is set, enabling the FWD FET of the servo preamplifier

- The negative going demodulator output signal is applied through the FWD FET to the

non-inverting input of the servo preamplifier whose negative output provides more reverse drive

- The carriage then moves into a null or zero volt position

- As the carriage passes the null the demodulator output swings positive

- The positive voltage, applied through FWD FET to the non-inverting input of the operational amplifier, produces forward drive voltage to stop the carriage at the desired cylinder

- The positioning systems maintains this balance during detent
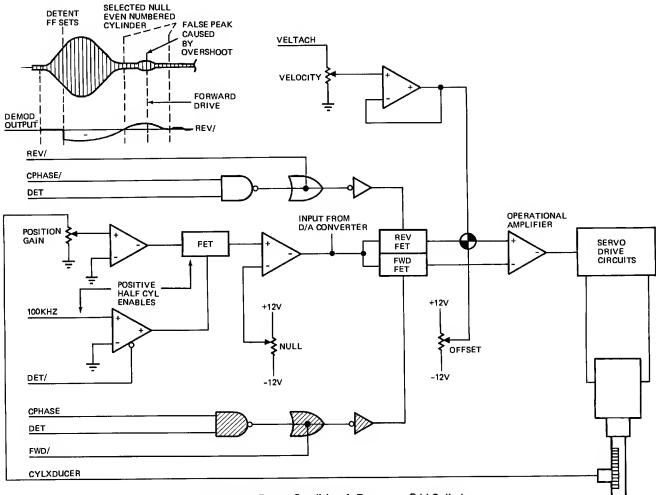
Figure 3-70. Detent Condition 4, Reverse to Odd Cylinder

READ/WRITE SYSTEM

The read/write system provides the means of reading or writing data on a specified surface of a rotating disk pack as directed by the controller. The read/write system includes the following major elements:

- Head Address Control Logic — encodes head address lines from controller to select a left head and right head pair and enables the left or right read/write circuits

- Write Circuits — generate current through one of twenty read/write heads, causing the disk to be magnetized in accordance with digital write data from the controller

- Read Circuits — amplify and condition voltage changes (playback) from read/write head to the form in which it was sent from the controller during the write operation
- Read/Write Heads — common head used for reading and writing:
  1. During write operation, provides means of magnetizing disk surface in accordance with write current from write circuits and provides straddle erase for track separation
  2. During read operation provides means of sensing magnetic field changes on disk surface

DISK PACK ORGANIZATION AND HEAD ARRANGEMENT

The disk pack, as shown in Figure 3-71, contains 20 recording surfaces, with each surface divided into 203 cylinders. One head at one specific detent position defines a circle on the disk surface as it rotates: a circle of recorded data is called a track.
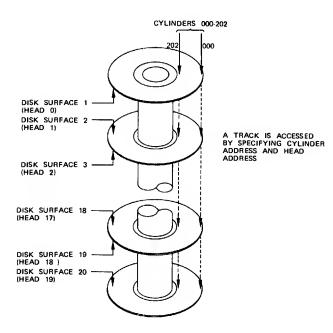
Figure 3-71. Disk Pack Organization

Recorded areas are addressed by selecting a single track which is the intersection of a specific cylinder and disk surface.

There are 4060 tracks. A track address consists of the cylinder address and the head address. When the controller accesses a specific track, the read/write heads are moved to the required cylinder location. The head address specifies the disk surface to be accessed.

The heads are arranged in a vertical plane so that 20 tracks are available for access without any head carriage movement; that is, when read/write head 00 is positioned at cylinder 005 of its disk surface, read/write heads 01 through 19 are also positioned at cylinder 005 of their respective surfaces.

HEAD ADDRESS CONTROL LOGIC

The head address control logic includes a 5-bit head address register, a 4-to-10 line decoder, and ten head select switches. Figure 3-72 is a simplified block diagram of the head address control logic.
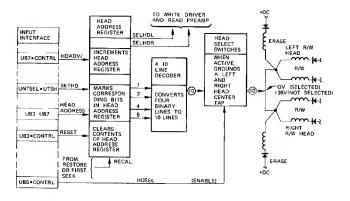
Figure 3-72. Head Address Control, Simplified Block Diagram

Figure 3-73 shows the head address control logic.

Head Address Register

The head address register (Figure 3-74) contains five flip-flops to store the binary head address from the controller.

The states of four of the flip-flops (HAR2, HAR4, HAR8, and HAR16) are applied to the 4-to-10 line decoder to select a left and right head pair. The states of the two least significant bits (HAR1 and HAR2) are applied to select logic for selection of a left or right read preamp and write driver.

Clearing Head Address Register — The head address register must be cleared prior to each loading or the register contents will be the inclusive OR of each loading. For example, if the head address register contains a seven (0111) and is loaded with an eight (1000), without first being cleared, the stored result will be a fifteen (1111).
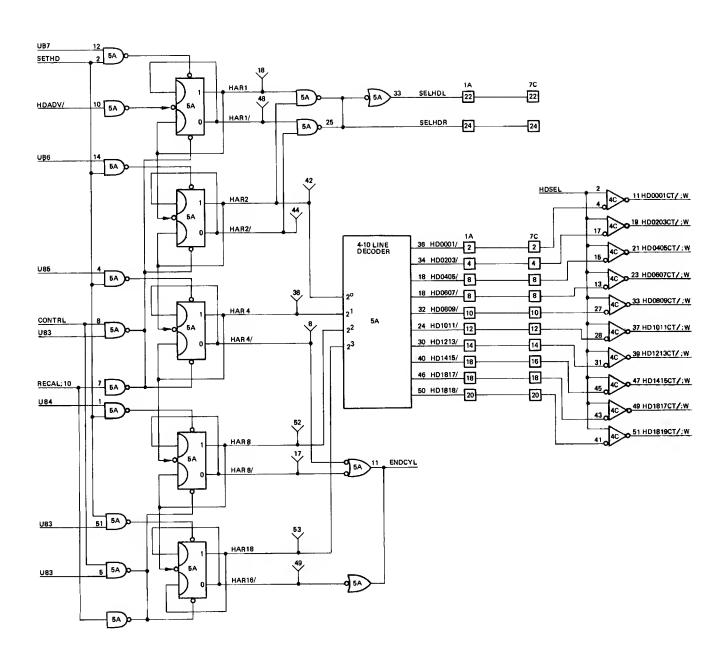
Figure 3-73. Head Address Control, Logic Diagram
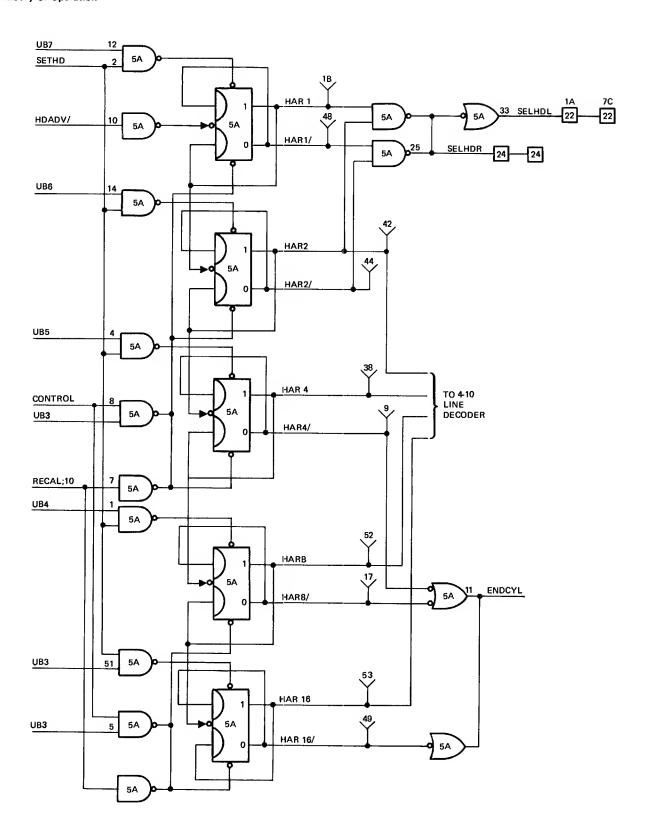
Figure 3-74. Head Address Register Logic

The head address register can be cleared in the following ways:

- As a result of a first seek or restore operation, (RECAL;10 active)
- During a program seek prior to loading the head address register for a subsequent read/write operation (UB3·CONTRL)

Loading Head Address Register — The head address register is loaded during a program seek, prior to a read/write operation. To load the head address register, the controller sends the head address on UB3-UB7 and set head tag (UTSH). UTSH is ANDed with UNTSEL (drive selected) to produce SETHD (set head). SETHD is ANDed with the states of UB3-UB7 to mark the corresponding bits in the head address register. The states of the head address register are then applied to the 4-to-10 line decoder and left and right head selection logic.
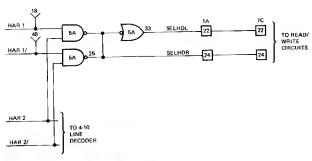
Left and Right Read/Write Circuit Selection — The states of the two least significant bits (HAR1 and HAR2) are applied to left and right selection logic to select the left or right driver (write operation) or the left or right read preamp (read operation). Figure 3-75 is a matrix showing the states of HAR1 and HAR2 and the left and right selection logic.

Incrementing Head Address Register — Each flip-flop in the head address register is connected to change state on the negative transition of its clock input. The set output of each lower-order bit is connected to the clock input of the next higher-order bit, except for HAR1. The clock input for HAR1 is HDADV/. When the controller increments the head address register, the following occurs:

- The controller sends UB7 and UTCC
- The interface logic develops HDADV/ from UB7·UTCC
- Trailing edge of HDADV/ low is applied as the clock input to HAR1

For the purpose of explaining the incrementing process, assume the head address register contains a three (0011).

- HAR1 set, HAR2 set, and HAR4 reset
- On the negative transition of HDADV/ HAR1 changes state (HAR1 reset)
- Low clock input to HAR2 resets HAR2
- Low clock input to HAR4 sets HAR4
- The end result is (0100) HAR1 reset, HAR2 reset, and HAR3 set which is a four (0100)

16 HAR16	8 HAR8	4 HAR4	2 HAR2	1 HAR1	SELHDL	SELHDR
0	0	0	0	0	00	
0	0	0	0	1		01
0	0	0	1	0		02
0	0	0	1	1	03	
0	0	1	0	0	04	
0	0	1	0	1		05
0	0	1	1	0		06
0	0	1	1	1	07	
0	1	0	0	0	08	
0	1	0	0	1		09
0	1	0	1	0		10
0	1	0	1	1	11	
0	1	1	0	0	12	
0	1	1	0	1		13
0	1	1	1	0		14
0	1	1	1	1	15	
1	0	0	0	0	16	
1	0	0	0	1		17
1	0	0	1	0		18
1	0	0	1	1	19	

Figure 3-75. Left and Right Selection Logic and Truth Table

End of Cylinder Logic — The outputs of HAR4, HAR8 and HAR16 are connected to logic which determines when the contents of the head address register is greater than 19. Figure 3-76 shows the logic.
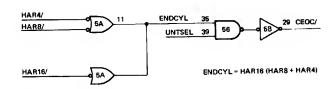
Figure 3-76. End of Cylinder Logic

When the count is greater than 19, ENDCYL goes high and CEOC/ low is available to the controller to indicate an invalid head address.

4-to-10 Line Decoder

The states of HAR2, HAR4, HAR8, and HAR16 are applied to the 4-to-10 line decoder. With respect to the decoder, the four bits represent a binary coded 1, 2, 4, and 8 respectively. The decoder converts the states of the four head address register bits to one of ten preselection lines. The ten lines are connected to the head select switches. An input in binary greater than 9(1001) results in all outputs off (high).

Head Select Switches

There are ten head select switches (Figure 3-77). Each switch is preselected by its corresponding output from the 4-to-10 decoder, prior to a read or write operation.
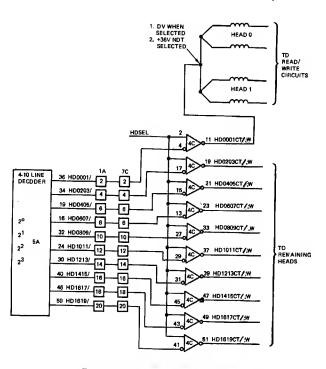
Figure 3-77. Head Select Switches

When the read/write operation is initiated the following occurs:

- The controller sends UB5 and UTCC (HDSEL)
- HDSEL is applied to all ten head select switches
- The switch with the active decoded input, from the decoder, applies ground to the center tap of a left and right head pair
- The output of the other nine switches remain at +36 volts, disabling the other 18 read/write heads

Error Conditions — The head select switches include logic to detect the following error conditions:

- HDSEL high and no head-pair selected
- HDSEL high and more than one head-pair selected
- HDSEL low and a head-pair selected

WRITE CIRCUITS

The write circuits are contained on the write driver module and left and right read preamplifier modules. The write circuits perform the following major functions:

- Receive and condition write data from the controller
- Supply current to the write and erase coils
- Disable the read circuits during a write operation
- Decrease write current when a cylinder greater than 127 is specified

Initiating a Write Operation

During a program seek, prior to the write operation, the following occurs:

- The head address register is loaded
- The left or right write driver circuitry is enabled by the states of HAR1 and HAR2

After the positioning system enters the detent mode, the controller may initiate a write operation by providing the following:

- UB0·UTCC = WRGATE/
- UB4·UTCC = ERGATE/
- UB5·UTCC = HDSEL
- Data to be written

Enable Switches

The input interface develops WRENA (write enable), ERENA (erase enable) from WRGATE/ and ERGATE/. WRENA/ and ERENA/ are applied to the write driver circuitry. Figure 3-78 is a simplified schematic of the write driver module circuits.

WRENA/ low, turns on Q12 and Q13 (write enable switch). ERENA/ low turns on Q2 and Q5 (erase enable switch). The write enable switch and erase enable switch provide operating bias for the write and erase current drivers, respectively. Normally the unsafe current switch (Q4) is on, supplying operating bias to the erase switch and write switch. If an unsafe condition occurs, Q4 turns
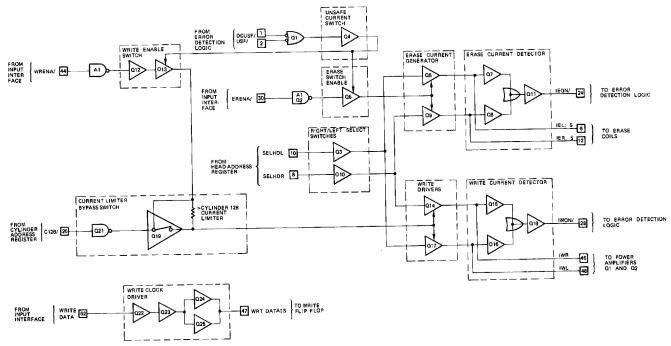
Figure 3-78. Write Driver Circuits, Simplified Schematic

off and removes operating bias to the erase switch and write switch, thereby terminating the write operation.

The states of SELHDL and SELHDR provide bias for either the left or right erase current driver and write current driver.

Erase Current Flow

The output of the enabled erase current driver is applied to the erase coil and the erase current detector.

The erase current detector is used by the unsafe logic to detect when erase current is flowing. Because the center taps of the enabled head pairs are at ground and because only one current driver is enabled, current flows from ground through an erase coil, through the enabled erase current driver, to the positive source (+36 volts).

Write Current Flow

Write current flow is similar to erase current flow. When a write driver is turned on, the write current detector sends IWON/ (write current on) to the unsafe logic. Figure 3-79 shows write current flow.

Current flow is from center tap ground through one write coil, through one power amplifier, through the enabled write driver to the positive source (+36 volts).

The unsafe detection logic provides an unsafe indication if the write current and erase current are not turned on simultaneously. Because of the straddle erase scheme, an unsafe condition is detected if the erase current is not turned off within 60 microseconds after write current.
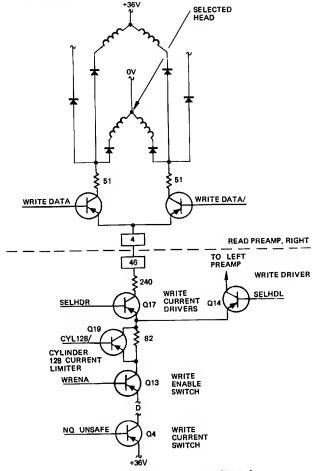
Figure 3-79. Write Current Flow (Right), Simplified Schematic Diagram

Cylinder 128 Bypass — As data is written closer to the center of the disk, bit packing density is increased and the heads fly closer to the disk surface due to decreased rotational velocity. If the write current is not decreased, the magnetic field will saturate the head during playback, thus decreasing frequency response and resulting in possible head errors. To prevent this condition, write current is decreased at cylinder addresses above cylinder 128. When C128/ goes low, Q19 turns off and switches a current limiting resistor in the write head current flow path.

Recording Format

The standard model 114 disk drive utilizes the following recording format conventions:

- Data-Bit Cell Time — the time between clock pulses
- Data-One — a data-one is represented by a flux change 200 nanoseconds after a clock bit
- Data-Zero — a data-zero is represented by the absence of a flux change after a clock bit

When a data-one is written, there are two flux changes. The flux change caused by the clock bit and the flux change caused by the data-bit immediately following the clock bit.

When a data-zero is written, there is only the flux change caused by the clock bit.

When a write operation takes place, the controller sends a serial pulse train as shown in Figure 3-80.
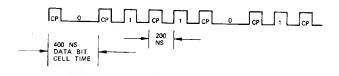
Figure 3-80. Pulse Train From Controller

In the standard model, the pulse train is routed through a bi-directional coax used for both write data and read data and is applied to the write clock driver (Figure 3-81). All other model units incorporate separate coax lines for read and write data transfers.
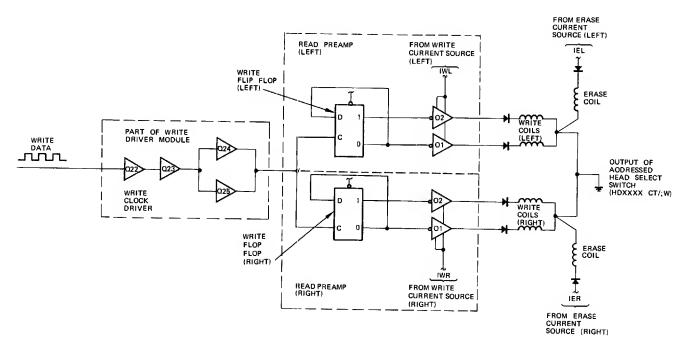
Figure 3-81. Write Flip-Flop and Associated Circuits

The write clock driver reshapes the double frequency write data and applies it to the clock input of both left and right write flip-flops. The flip-flops are wired so that each positive transition of the write data cause them to change state. The changing state of the flip-flop alternately enables amplifier Q1 and Q2, enabling current to flow through one coil and then the other.

Figure 3-82 shows the biasing that allows current to alternate through each write coil. Also shown, is a write data bit pattern and the resultant write flip-flop output. Because Q1 and Q2 do not alter the bit pattern, their outputs will essentially be the same bit pattern as the flip-flops.
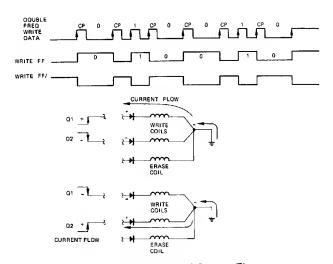
Figure 3-82. Write Coil Current Flow

Read/Write Head Characteristics During Writing

The read/write head, when driven by current, provides a magnetizing force to the ferrous rotating disk surface. The head is essentially an electromagnet capable of switching polarity at high frequencies and capable of concentrating a magnetizing force on a very small area of the recording surface. The magnetizing force is sufficient enough to change a previously recorded field to the opposite polarity. The recording head (Figure 3-83) consists of two coils wound on a split ferrite core.
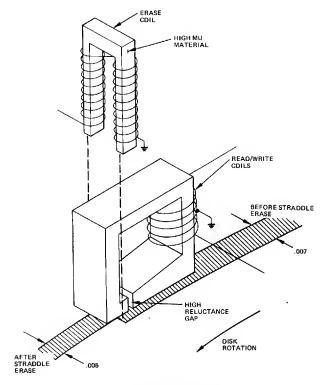
Figure 3-83. Read/Write Head

Erase Coil — The erase coil is wound on both legs of a U-shaped high MU core and physically straddles the read/write head core.

The radial track density is 100 tracks per inch; that is, .010-inch per track. When a constant dc current is driven through the erase coils, the written track width is erased from .007-inch to .005-inch to provide track separation and eliminate track-to-track cross talk. Figure 3-84 shows the straddle erase scheme.
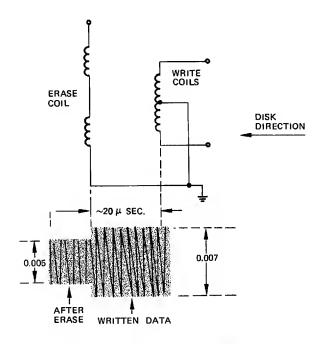
Figure 3-84. Straddle Erase

The erase coil is physically located .045-inches behind the write coil. With respect to disk rotation this is approximately 20 microseconds.

Erase current must remain on at least 20 microseconds after write current is disabled or the last portion of the track will not be erased.

READ CIRCUITS

The read circuits are contained on the left and right preamplifiers, the read amplifier, and the crossover detector. During the read operation the circuits perform the following functions:

● Convert the selected read/write head into a magnetic field sensor
● Amplify and shape the playback signal to a form useable by the controller
● Control the read signal output to the controller

Initiating a Read Operation

After the positioning system enters the detent mode, the controller may initiate a read operation by providing the following:

- UB1·UTCC = RDGATE
- UB5·UTCC = HDSEL

RDGATE disables the squared oscillator and enables the final output stages of the read circuits. The squared oscillator is disabled to minimize noise during the read operation.

Enabling Coupling Transformer

Since a write operation is not being performed, WRENA/ is high. WRENA/ high enables the coupling transformer network, as shown in Figure 3-85.
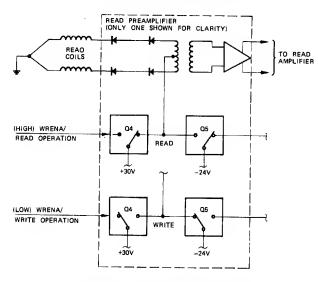
Figure 3-85. Coupling Transformer Bias

During a read operation, WRENA/ high causes Q4 to switch +30 volts to the coupling transformer center tap, forward biasing the read head diodes and allowing the head coils to sense the magnetic fields recorded on the disk surface. During a write operation, WRENA/ low causes Q5 to switch -24 volts to the coupling transformer center tap reverse biasing the diodes. This decouples the transformer and allows the heads to be used for writing.

Read/Write Head Characteristics During Reading

The head coils are connected in series with a 30 k ohm resistor to +36 volts dc, resulting in approximately 1-2 milliamps through each coil. The current flow generates a small flux field in each core half. Since the magnetic

poles of the core halves are opposing, a small external field is produced at the gap. The disturbance of the field by the recorded magnetic field causes a change in core flux and very small voltage of 1 to 2 millivolts is induced in the coil. The coupling transformer turns ratio is 1:1 and provides no signal gain. The read preamplifier amplifies the sensed signal and applies it to the read amplifier circuit.

Read Preamplifier Selection

As in the write operation, when a head is selected during read, two head center taps are also grounded (left and right), allowing the outputs of both read preamplifiers to be applied to the read amplifier circuits. The states of SELHDL and SELHDR enable one input and disable the other input. Figure 3-86 shows the select gates.
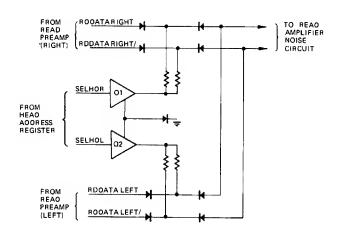
Figure 3-86. Read Preamplifier Selection

If SELHDR is high, SELHDL is low. SELHDR turns on Q1 and forward biases the isolation diodes. Q2 turns off and reverse biases the RDATALEFT diodes. To enable RDATALEFT, Q2 turns on and Q1 turns off. The selected output is then applied to the read amplifier. Figure 3-87 shows the different stages of shaping and amplification as the playback signal is applied to each stage of the read amplifier and crossover detector circuits.

Read Amplifier and Crossover Detector

At the top of Figure 3-87 is the double frequency bit pattern from the write circuit power amplifiers. Immediately below is the bar magnet representation of the data recorded on the disk surface. The next waveshape (SENSED DATA) shows the corresponding signal obtained from the read coils.
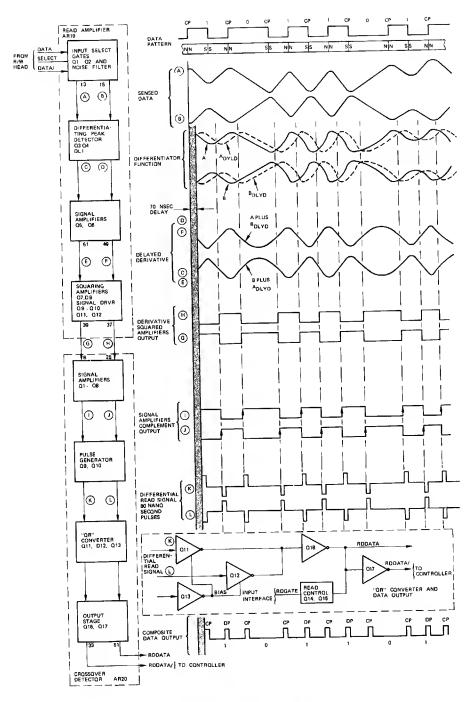
Figure 3-87. Read Circuit Waveforms

- The sensed data is irregular because of read coil response and the magnetic characteristics of the disk surface
- The sensed data does not have a zero reference level and the amplitude is not fixed
- The negative and positive going peaks correspond to the transitions of the clock and data pulses

It is the task of the read amplifier and crossover detector circuits to restore the sensed data back to a serial pulse train for use by the controller. The following occurs during a read operation:

- The sensed data is applied to two 2.2 μh chokes (noise filter)

- The output of the noise filter is applied to a differentiator and peak detector stage, comprised of Q3, Q4, and delay line DL1
- Q3, Q4, and DL1 delay each side of the sensed data by 70 nanoseconds and sum the delayed signal with the opposite polarity signal
- The resultant is the sensed data, base line corrected (restored to a zero reference level) and fixed in amplitude. The baseline crossovers correspond to the peaks of the sensed data which in turn corresponds to the double frequency clock pulses and data-one pulses
- The outputs of Q3 and Q4 are applied to signal amplifiers Q5 and Q6 which amplify the resultant signal and apply it to squaring amplifier Q7 and Q8

- The squaring amplifier provides a digital pulse train that is the complement of the input and that switches state at each base line crossover
- Q9 through Q12 increase the signal strength
- The output of the squaring amplifier is applied to pulse generators Q9 and Q10
- Q9 and Q10 provide differential pulses that are triggered by the positive- and negative-going signal amplifier outputs
- The differential pulses are applied to OR converter Q11-Q13
- The OR converter performs a logical OR of only the positive-going differential signals and applies the ORed outputs to the output stage
- The OR converter outputs are enabled back to the controller by RDGATE high. Figure 3-88 is a flow diagram of the read/write operation
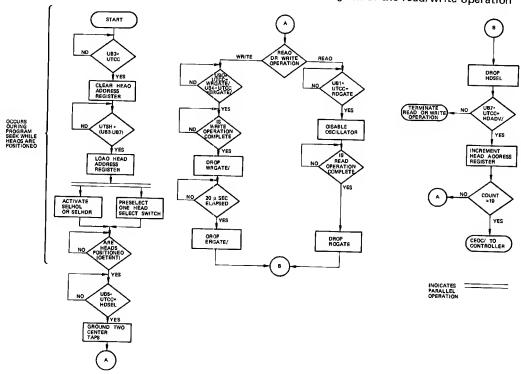
Figure 3-88. Read/Write Operation, Flow Diagram

ERROR DETECTION

The error detection logic detects those conditions which can degrade disk drive operation or alter the integrity of recorded data. The error detection logic is divided into three major categories:

- Emergency retract conditions
- Unsafe conditions during a read or write operation
- Program seek error conditions

The error detection logic (Figure 3-89), includes monitor gates and flip-flops for latching error conditions.

EMERGENCY RETRACT CONDITIONS

An emergency retract is caused by any condition which can damage the read/write heads and/or the disk surface. The following is a list of emergency retract conditions:

- During a seek operation, the carriage hits the end stop (off rack when ready)
- During a first seek or restore, unable to achieve detent after one second (seek error)
- Losing 30 percent of speed while the heads are extended
- 100 kHz oscillator failure when disk drive is ready
- Loss of any dc supply voltage
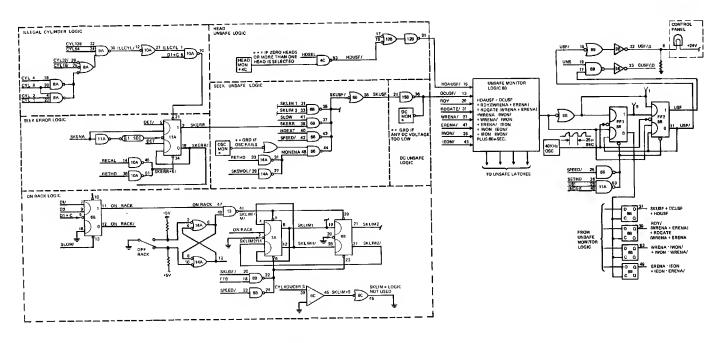
Figure 3-89. Error Detection Logic

Figure 3-90 shows the emergency retract monitor logic.
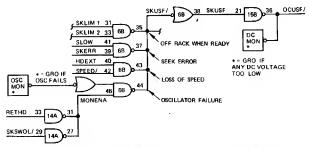
Figure 3-90. Emergency Retract Monitor Logic

Off Rack When Ready

During a first seek or restore operation, the carriage is driven to the end stop and then in reverse back to cylinder zero. As the carriage passes cylinder 201, the ON RACK flip-flop sets. Figure 3-91 shows the ON RACK logic.

Figure 3-91. ON RACK Logic
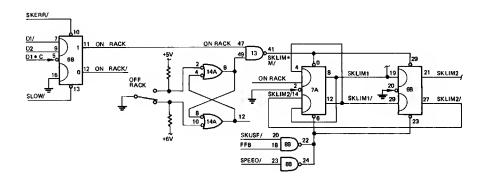
When the carriage is driven to the end stop, the difference counter is equal to 204. As the carriage is driven in reverse, the cylinder transducer passes the rack. Difference clocks (DI*C) are generated and decrement the difference counter. When the difference counter is decremented to 202, the set inputs to the ON RACK flip-flop are active (D1/ and D2). At the next difference clock (cylinder 201) the ON RACK flip-flop sets and remains set until a restore is issued or the heads are retracted.

When the ON RACK flip-flop sets it enables the off rack latch to monitor the off rack switch. In the event of an error, such as the wrong difference being calculated, the carriage attempts to seek to the cylinder position. If the carriage goes to the end stop, the off rack microswitch contacts close and the off rack latch sets. The SKLIM1 and SKLIM2 flip-flops are then marked, thus indicating a seek unsafe (SKUSF/) and causing an emergency retract.

Seek Error

The set inputs to the SKERR flip-flop (Figure 3-92), are connected to DET/ and SKENA. During first seek or restore, SKERR is clocked one second after SKENA is set.

If SLOW and SKERR are on at the same time, a seek unsafe exists and an emergency retract will take place.
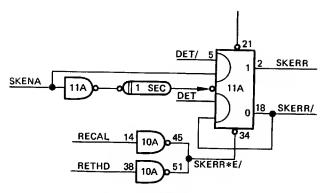
Figure 3-92. Seek Error Logic

Loss of Speed with Heads Extended

During first seek, when the heads are extended, the heads extended microswitch transfers and the heads extended latch is set. If the heads are extended and the disk pack rotational speed drops 30 percent, an emergency retract will occur to protect the heads and the disk pack.

100 KHZ Oscillator Failure

When the 100 kHz oscillator fails, the failure is detected by the oscillator monitor circuit (Figure 3-93). If the oscillator operates properly, the monitor output (SKUSF/) is high. If the oscillator fails, SKUSF/ goes low and initiates an emergency retract.
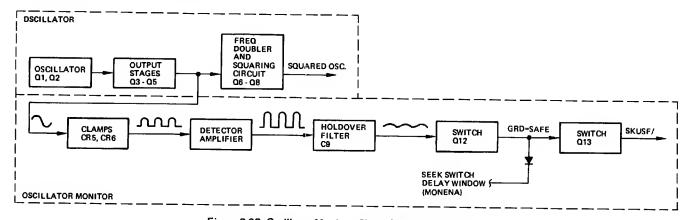
Figure 3-93. Oscillator Monitor, Simplified Block Diagram

During normal operation, the oscillator is supplying a 100 kHz, 5-volt peak-to-peak, input signal to the monitor circuit. Two clamping diodes (CR5 and CR6) and detector amplifier (Q10, Q11) convert the 100 kHz signal to a pulsating dc. The pulsating dc is then detected and amplified by Q10 and Q11, and filtered by capacitor C9. The discharge time of the filter is considerably less than the 100 kHz cycle time; thus, as long as the 100 kHz signal is correct, the capacitor remains charged. The filtered signal is then applied to Q12. If the 100 kHz is

correct Q12 conducts to ground, applying ground to the base of Q13. Q13 remains off and SKUSF/ is high. If a failure occurs, Q12 turns off and Q13 turns on. Q13 grounds SKUSF/ and an emergency retract occurs.

At the start of first seek, when the heads are being extended, the monitor is disabled by turning Q13 off (SKUSF/ high) during the 190-millisecond seek switch delay time (MONENA low). When the heads are retracted, RETHD high disables the oscillator monitor (MONENA low).

Loss of DC Voltages

A dc power monitor circuit (Figure 3-94), monitors the +5-, +24-, -24-, +36-, and +45-volt supply voltages. If any of the dc supply voltages fall below a predetermined level, the power monitor circuit grounds DCUSF/ and an emergency retract is initiated. The power monitor circuit includes the following major elements:
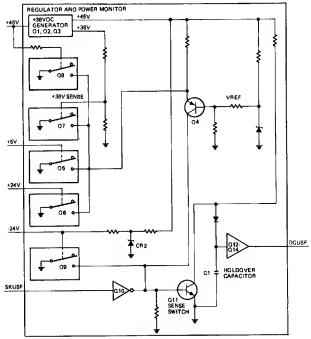
Figure 3-94. Power Monitor Circuit

- +36V dc generator and regulator
- Five voltage sensing circuits
- Reference voltage circuit
- Sense switch circuit
- Holdover capacitor

If the supplies are operating normally, the outputs from the sense circuits are high, causing transistor Q4 to conduct. Transistor Q4 and associated components serve as a reference voltage circuit. If Q4 conducts, Q11 receives base current and also conducts. Transistor Q11 functions as a sense switch. When the power supplies are up, the sensed outputs are high and Q11 conducts. When Q11 conducts, it holds Q12, Q13, and Q14 off.

If a supply voltage drops below a predetermined level the respective sense switch turns on and switches ground to Q4. Q4 turns off which turns Q11 off. As Q11 turns off, the holdover capacitor starts to charge. After 3 milliseconds, the holdover capacitor is charged and the voltage is sufficient to turn on Q12, Q13 and Q14. The 3 millisecond charge time is provided for noise rejection. A transient noise spike, by circuit definition, is any supply voltage decrease for less than 3 milliseconds. That is, if a supply voltage decreases for less than 3 milliseconds, the

holdover capacitor never fully charges and Q12, Q13, and Q14 remain off. DCUSF/ remains high. If the power supply output decreases for greater than 3 milliseconds, Q12, Q13, and Q14 conduct, an unsafe is indicated (DCUSF/ low), and the holdover capacitor discharges for approximately 150 milliseconds.

While the holdover capacitor is discharging, Q12, Q13, and Q14 cannot turn off. Thus, if a power supply output decreases for at least 3 milliseconds, a dc unsafe will be indicated for 150 milliseconds. Since DCUSF/ low is applied to the servo system emergency retract circuits, DCUSF/ has to be low for approximately 150 milliseconds to retract the heads from their furthest position. If the power supply recovers within the 150 millisecond window, the holdover capacitor charge is enough to turn off Q12, Q13, and Q14. If after 150 milliseconds the supply is still low, Q12, Q13, and Q14 remain on, indicating an unsafe condition.

UNSAFE READ OR WRITE CONDITIONS

Logic is provided to monitor certain illegal read/write conditions. The output of the monitor logic gates are connected to a common collector ORed point. If the incorrect conditions exist, the OR point goes low and indicates an unsafe condition. In addition, the emergency/retract conditions are also connected to the OR point. Figure 3-95 shows the unsafe monitor logic.
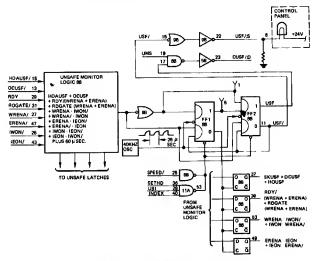
Figure 3-95. Unsafe Monitor Logic

The following is a list of unsafe read/write conditions that can occur as a result of malfunctions from the controller, input interface logic, or read/write circuits.

- Disk drive not ready and write enable or erase enable active — RDY/(WRENA + ERENA)
- Read gate active and write enable or erase enable active — RDGATE(WRENA + ERENA)
- Write enable active and no write current detected — WRENA · IWON/

- Write current detected and erase enable inactive — IWON · WRENA/
- Erase enable active and no erase current detected — ERENA · IEON/
- Erase current detected and erase enable inactive — IEON · ERENA/
- Write current detected and no erase current detected — IWON · IEON/
- Erase current remains on more than 60 μseconds after fall of write current
- Erase current detected and no write current detected — IEON · IWON/

A read or write unsafe condition can also be caused as a result of a head select switch malfunction.

Head Select Switch Malfunction

When the head address register is loaded and HDSEL is high, the head select switches (Figure 3-96) switch the center tap of a left and right read/write head pair from +36V dc to ground.

Logic is provided to detect the following illegal conditions.

- HDSEL high and no head pair selected
- HDSEL high and more than one head pair selected
- HDSEL low, and a head pair selected

Decoder outputs HD0001/ through HD1819/ are applied to 10 identical head select drivers through identical inverter gates. The bias for the head select drivers is furnished on a common line through transistor Q2. When HDSEL is high, transistor Q2 is turned on, and the common bias line supplies head select drivers (Q9 through Q18) with an enabling bias voltage. During a safe operation, a head select driver should not be turned on when HDSEL is low. If a driver is on with HDSEL low, an unsafe condition is detected.

A sense amplifier (transistor Q8) and head select drivers Q9 through Q18 are connected to a common output line. Q8 does not receive bias through the common bias line, but operates independently, as determined by the state of HDSEL. The purpose of Q8 is to simulate a head pair being selected when HDSEL is low; when HDSEL is low, Q8 is turned on; when HDSEL is high, Q8 is turned off.
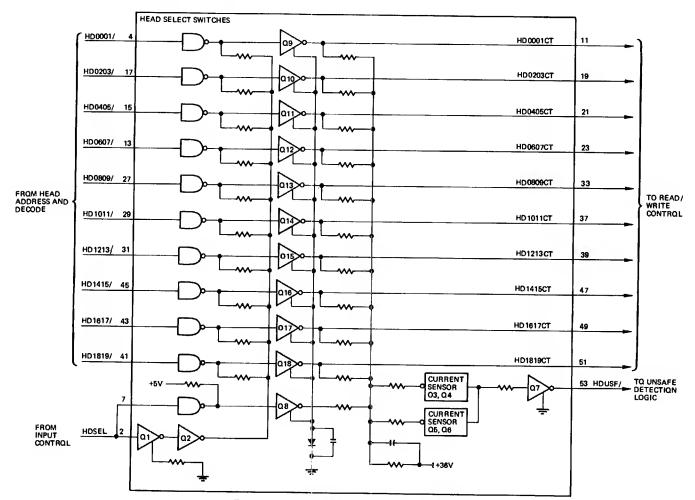
Figure 3-96. Head Select Switches, Logic Diagram

Sense amplifier Q8 and head select drivers Q9 through Q18 have load resistors of identical value. Each circuit draws an equal current and drops an equal voltage. When the circuit is operating normally, only the selected driver conducts. If HDSEL is high Q8 is off and the selected driver is on. If HDSEL is low, Q8 is on, simulating a head pair has been selected and bias amplifier Q2 is off. If for some reason one of the head select drivers conducts with simulator Q8 on, the voltage on the common output line falls to a lower level.

Connected to the common output line are two current sensors. Transistors Q3 and Q4 comprise one sensor and transistors Q5 and Q6 comprise the other sensor. During a safe condition the output of both sensor circuits are low. That is, as long as either the sense amplifier (Q8) or one of the head select drivers conducts, the current sensor circuits remain off. If more than one head pair has been selected at HDSEL time, Q3 and Q4 operate in conjunction to sense a greater current drain. If a head pair is not selected at HDSEL time, Q5 and Q6 operate in conjunction to sense an insufficient current drain.

HDSEL High and No Head Pair Selected — If HDSEL is high and no head pair is selected (Figure 3-97), an insufficient amount of current is being drawn. With a head pair not selected and HDSEL high, a load resistor is not switched into the circuit; therefore, less current is drawn. Q3 and Q4 are biased to detect less current drain. Q4 on then turns Q7 on and HDUSF/ goes low indicating an unsafe condition.
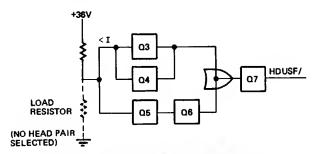
Figure 3-97. HDSEL High and No Head Selected

HDSEL High and Multiple Head Pairs Heads Selected — If HDSEL is high and more than one head pair has been selected (Figure 3-98), an excessive amount of current is being drawn.
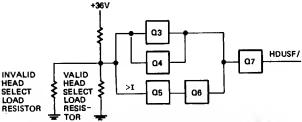
Figure 3-98. HDSEL High and Multiple Head Selected

Two load resistors are in the circuit; one for the selected head pair and one for the invalid head pair. The resistance is halved, therefore the current increases to an excessive amount. When an excessive amount of current is drawn, Q5 turns on and Q6 turns off. HDUSF/ goes low to indicate an unsafe condition.

HDSEL Low and a Head Pair Selected — If HDSEL is low Q8 is turned on and its load resistor and the selected head pair load resistor are both in the circuit. Therefore an excessive amount of current will be drawn and the circuit will function the same as HDSEL high and multiple head pairs selected.

LATCHING UNSAFE (SELECT LOCK) CONDITIONS

By logic definition, emergency retract conditions and read/write unsafe conditions are defined as unsafe conditions (USF). There are two types of unsafe cards: the AL15 and AL48. The AL15 will be described first, followed by the AL48 differences.

AL15 Unsafe Detection

FF1 and FF2 (Figure 3-99), provide a means of latching unsafe conditions. Both flip-flops are clocked by a 40 kHz oscillator. The oscillator provides a 25 microsecond clock period. If an unsafe condition exists, FF1 sets with one clock pulse from the oscillator.
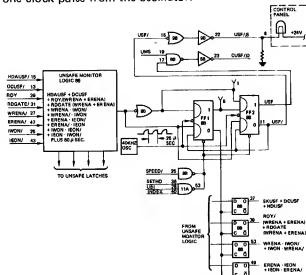
Figure 3-99. Latching Unsafe Conditions (AL15)

If the unsafe condition still exists at the next clock pulse, FF2 sets. If the unsafe condition is less than two clock periods, FF1 sets on the negative transition of the first clock and resets on the negative transition of the second clock. If FF2 sets, USF/ low develops ground to light the control panel SELECT LOCK indicator and disable the input control logic and write driver circuit.

USF(FF2) is ANDed with UMS (Unit Module Select) from the controller; when the disk drive is selected and an unsafe condition exists, SELUSF/ goes low (selected unsafe) which develops CUSF/ low. CUSF/ low informs the controller that the disk drive is not safe for operation.

FF1 and FF2 can both be erased by either of two conditions: (1) loss of 70 percent of speed (SPEED/) or (2) SETHD · UB1 · INDEX. The latter condition is used by some controllers during particular diagnostic routines to reset an intentional SELECT LOCK.

SPEED/ can be obtained by powering down the disk drive; thus an intermittent SELECT LOCK can be cleared by powering down the disk drive. Solid select locks require repair of the malfunction before the condition can be cleared.

The reset output of FF1 is connected as a clock input to four latches. The data input to each latch is connected to specific unsafe monitor logic. When FF1 sets, as a result of an unsafe condition, the negative going reset side of FF1 prevents the latch outputs from following the data inputs. The latch that is connected to the unsafe condition remains on, and the remaining three latches remain off as they did not detect an unsafe condition. If the unsafe condition clears before the next clock, FF1 resets on the next clock and the latch holds the unsafe condition. If the unsafe condition still exists and FF2 is set, then the specific error condition remains latched until the drive is powered down.

AL48 Unsafe Detection

The differences between the AL15 and the AL48 (Figure 3-100) are in the methods of clocking the four latches and transient elimination.
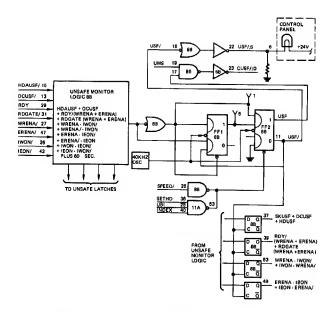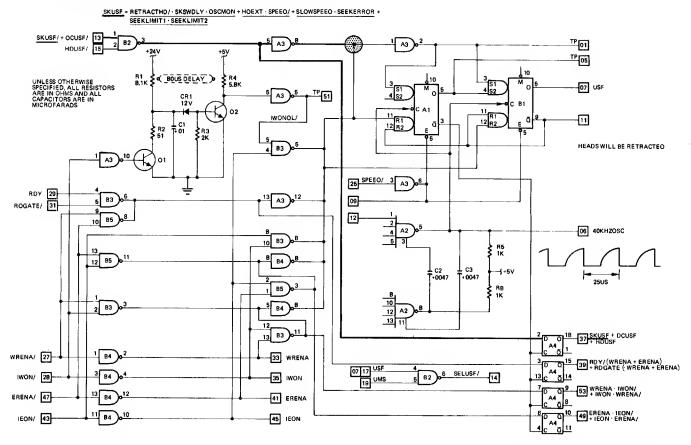
Figure 3-100. Latching Unsafe Conditions (AL48)

In the AL15, the latches clock from the reset output of the first unsafe flip-flop, whereas in the AL48 the latches clock from the reset output of the second unsafe flip-flop. The major functional difference between the AL15 and the AL48 is that losing speed erases both flip-flops on the AL15, while on the AL48, the erase of the first flip-flop is tied to the error set input. Thus, if there is a transitory error condition, the first flip-flop will be erased upon clearing of the transit condition. Through this scheme the possibility of obtaining an unsafe indication on two successive noise transients which coincide with the 40 kHz oscillator is eliminated.

Figure 3-101 through 3-111 show the unsafe logic and the eleven unsafe conditions. Included are logic equations expressing each condition.

$$USF = \underline{SKUSF} + \underline{DCUSF} + \underline{HOUSF} + \underline{RDY/(WRENA + ERENA)} + \underline{RDGATE\ (WRENA + ERENA)} +$$
$$\underline{IWON/\cdot IEON} + \underline{IEON/\cdot IWON} + \underline{ERENA\cdot IEON/} + \underline{IEON\cdot ERENA/} + \underline{WRENA\cdot IWON/} + \underline{IWON\cdot WRENA/}$$

$$\underline{SKUSF} = \underline{RETRACTHD/\cdot SKSWDLY\cdot OSCMON} + \underline{HOEXT\cdot SPEEO/} + \underline{SLOWSPEED\cdot SEEKERROR} +$$
$$\underline{SEEKLIMIT1\cdot SEEKLIMIT2}$$

UNLESS OTHERWISE
SPECIFIED, ALL RESISTORS
ARE IN OHMS AND ALL
CAPACITORS ARE IN
MICROFARADS

HEADS WILL BE RETRACTED

25US

The conditions which will develop a seek unsafe (SKUSF/) are described in the Emergency Retract Conditions paragraph. If SKUSF/ goes low, the common collector ORed point goes low and the condition is latched as described in the Latching Unsafe Conditions paragraph.

Figure 3-101. Unsafe Condition 1 (SKUSF)

USF = SKUSF + DCUSF + HDUSF + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +
IWON/·IEON + IEON/·IWON + ERENA·IEON/ + IEON·ERENA/ + WRENA·IWON/ + IWON·WRENA/

SKUSF = RETRACTHD/·SKSWDLY · OSCMON + HDEXT · SPEED/ + SLOWSPEED · SEEKERROR +
SEEKLIMIT1 · SEEKLIMIT2

The conditions which will develop a DC unsafe (DCUSF/) are described in the Loss of DC Voltages paragraph. If DCUSF/ goes low, the common collector ORed point goes low and the condition is latched as described in the Latching Unsafe Conditions paragraph.

Figure 3-102. Unsafe Condition 2 (DCUSF)

$$USF = \underline{SKUSF} + \underline{DCUSF} + \underline{HDUSF} + \underline{RDY/(WRENA + ERENA)} + \underline{RDGATE\ (WRENA + ERENA)} +$$
$$\underline{IWON/\cdot IEON/\cdot IEON/\cdot IWON} + \underline{ERENA\cdot IEON/} + \underline{IEON\cdot ERENA/} + \underline{WRENA\cdot IWON/} + \underline{IWON\cdot WRENA/}$$

$$SKUSF = \underline{RETRACTHD/\cdot SKSWDLY\cdot OSCMON} + \underline{HDEXT\cdot SPEED/} + \underline{SLOWSPEED\cdot SEEKERROR} +$$
$$\underline{SEEKLIMIT1\cdot SEEKLIMIT2}$$

The conditions which will develop a heads unsafe (HDUSF/) are described in the Head Select Switch Malfunction paragraph. If HDUSF/ goes low, the common collector ORed point goes low and the condition is latched as described in the Latching Unsafe Conditions paragraph.

Figure 3-103. Unsafe Condition 3 (HDUSF)

USF = SKUSF + DCUSF + HDUSF + RDY/(WRENA + ERENA) + ROGATE (WRENA + ERENA) +
IWON/·IEON + IEON/·IWON + ERENA·IEON/ + IEON·ERENA/ + WRENA·IWON/ + IWON·WRENA/

SKUSF = RETRACTHD/ · SKSWDLY · OSCMON + HOEXT · SPEED/ + SLOWSPEED · SEEKERROR +
SEEKLIMIT1 · SEEKLIMIT2

If for any reason WRENA or ERENA are active while RDY is active an unsafe condition will be detected as follows:

- When RDY/ goes low, gate B3-6 output goes high
- If WRENA/ goes low or ERENA/ goes low; gate B5-8 output goes high

- The two outputs are combined to form a dot-AND condition
- The high AND condition is applied to gate A3, causing pin 12 to go low (common collector ORed point)
- The condition is latched as described in the Latching Unsafe Conditions paragraph

Figure 3-104. Unsafe Condition 4 RDY/ (WRENA+ERENA)

$$USF = \overline{SKUSF} + \overline{DCUSF} + \overline{HDUSF} + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +$$
$$IWON/\cdot IEON + IEON/\cdot IWON + ERENA\cdot IEON/ + IEON\cdot ERENA/ + WRENA\cdot IWON/ + IWON\cdot WRENA/$$

$$SKUSF = RETRACTHD/\cdot SKSWDLY\cdot OSCMON + HDEXT\cdot SPEED/ + SLOWSPEED\cdot SEEKERROR +$$
$$\overline{SEEKLIMIT1\cdot SEEKLIMIT2}$$

Figure 3-105. Unsafe Condition 5 RDGATE (WRENA+ERENA)

If for any reason WRENA or ERENA are active while RDGATE is active, an unsafe condition will be detected as follows:

- When RDGATE/ goes low, gate B3-6 output goes high
- If WRENA/ goes low, or ERENA/ goes low gate B5-8 output goes high

- The two outputs are combined to form a dot AND condition
- The high AND condition is applied to gate A3, causing pin 12 to go low (common collector ORed point)
- The condition is latched as described in the Latching Unsafe Conditions paragraph

USF = SKUSF + OCUSF + HOUSF + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +
IWON/·IEON + IEON/·IWON + ERENA·IEON/ + IEON·ERENA/ + WRENA·IWON/ + IWON·WRENA/

SKUSF = RETRACTHD/·SKSWDLY·OSCMON + HOEXT·SPEEO/ + SLOWSPEED·SEEKERROR +
SEEKLIMIT1·SEEKLIMIT2

If erase current remains on for more than 60 microseconds after the write current is turned off, an unsafe condition is detected.
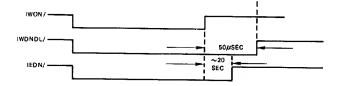
When write current is turned on the following occurs:

- IWON/ goes low and is inverted by gate A3
- Q1 turns on applying ground to the cathode of CR1, thereby turning Q2 off
- IWONDL/ goes low and the collector ORed point goes high

When write current is turned off the following occurs:
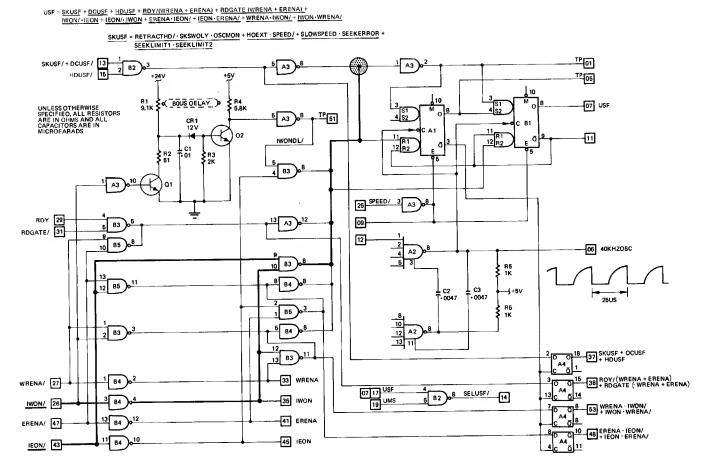
- IWON/ goes high, turning Q1 off
- C1 starts charging to 24 volts
- After 60 microseconds C1 charges to +12V and forward biases CR1

- Q2 turns on and IWONDL/ goes high
- If IEON/ is low at this time, the input to gate B3-4 is high, and the collector ORed point goes low
- The condition is not latched, but is implied by having a select lock and none of the latches set

The erase current turn off is controlled by the controller and in the standard 114 system nominal turn-off is 20 microseconds after write current is turned off.

Figure 3-106. Unsafe Condition 6 (IWON/·IEON)

USF = SKUSF + DCUSF + HDUSF + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +
IWON/·IEON + IEON/·IWON + ERENA·IEON/ + IEON·ERENA/ + WRENA·IWON/ + IWON·WRENA/

SKUSF = RETRACTHD/·SKSWOLY·OSCMON + HOEXT·SPEED/ + SLOWSPEED·SEEKERROR +
SEEKLIMIT1·SEEKLIMIT2
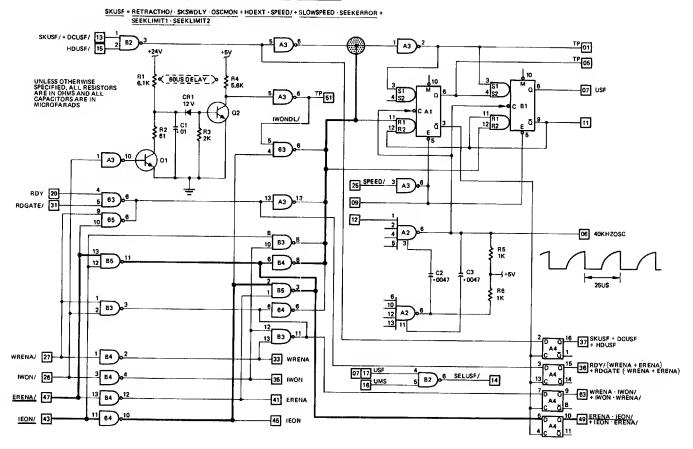
If write current is turned on and erase current is not turned on at the same time the following occurs:

- IWON/ goes low (write current on) and is applied to gate B3-10

- IEON/ remains high (erase current off) and is applied to gate B3-9
- The collector ORed point goes low and the condition is not latched

Figure 3-107. Unsafe Condition 7 (IEON/·IWON)

USF = $\overline{SKUSF} + DCUSF + HDUSF + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +$
$\overline{IWON/ \cdot IEON} + \overline{IEON/ \cdot IWON} + \overline{ERENA \cdot IEON/} + \overline{IEON \cdot ERENA/} + \overline{WRENA \cdot IWON/} + \overline{IWON \cdot WRENA/}$

$\overline{SKUSF} = \overline{RETRACTHD/ \cdot SKSWDLY \cdot OSCMON} + \overline{HDEXT \cdot SPEED/} + \overline{SLOWSPEED \cdot SEEKERROR} +$
$\overline{SEEKLIMIT1 \cdot SEEKLIMIT2}$

Figure 3-108. Unsafe Condition 8 (ERENA · IEON/)

If the erase current is enabled (ERENA) and no erase current is detected (IEON/) the following occurs:

- ERENA/ goes low and is applied to gate B5-13, causing B5-11 to go high
- IEON/ goes high and is applied to gate B4-11 causing output pin 10 to go low

- IEON is again inverted to a high at gate B5-3
- The two high outputs are ANDed at gate B4-9 causing the collector ORed point to go low
- The condition is latched as described in the Latching Unsafe Conditions paragraph

Figure 3-109. Unsafe Condition 9 (IEON • ERENA/)

If erase current is detected (IEON), but erase enable is not active(ERENA) the following occurs:

- IEON/ goes low and is applied to gate B5-12, causing output pin 11 to go high
- ERENA/ remains high and is inverted by gate B4-12

- The low level is inverted by gate B5-3
- The two high conditions are ANDed at B4-9
- The collector ORed point goes low and the condition is latched as described in the Latching Unsafe Conditions paragraph

USF = <u>SKUSF</u> + <u>DCUSF</u> + <u>HDUSF</u> + RDY/(WRENA + ERENA) + RDGATE (WRENA + ERENA) +
IWON/·IEDN + IEON/·IWON + ERENA·IEDN/ + IEDN·ERENA/ + WRENA·IWON/ + IWDN·WRENA/

SKUSF = RETRACTHD/·SKSWDLY·OSCMON + HDEXT·SPEED/ + SLOWSPEED·SEEKERROR +
<u>SEEKLIMIT1·SEEKLIMIT2</u>

SKUSF/ + DCUSF/ [13]
HDUSF/ [15]

UNLESS OTHERWISE
SPECIFIED, ALL RESISTORS
ARE IN OHMS AND ALL
CAPACITORS ARE IN
MICROFARADS

+24V   +5V

R1 8.1K   60US DELAY   R4 5.6K

CR1 12V   Q2

R2 51   C1 .01   R3 2K

Q1

A3 10

RDY [29]
RDGATE/ [31]

B3   B5

B5   B3   B4   B5   B4

B3

WRENA/ [27]   B4   [33] WRENA
IWON/ [26]   B4   [35] IWDN
ERENA/ [47]   B4   [41] ERENA
IEON/ [43]   B4   [45] IEDN

A3   A3   A3   B3   A3

IWONDL/

SPEED/ [25]   A3

[08]   [12]   A2   R5 1K

C2 .0047   C3 .0047   +5V   R8 1K

A2

S1 S2   M   O   C A1   R1 R2   E   Q

S1 S2   M   O   C B1   R1 R2   E   Q

TP [01]
TP [05]
[07] USF
[11]

[06] 40KHZOSC

25US

[37] SKUSF + DCUSF + HDUSF

[38] RDY/(WRENA + ERENA) + RDGATE (·WRENA + ERENA)

[53] WRENA·IWON/ + IWON·WRENA/

[48] ERENA·IEON/ + IEON·ERENA/

A4   A4   A4   A4

[07] [17] USF   B2   SELUSF/ [14]
[1B] UMS

If write enable is active (WRENA) and write current is
not detected the following occurs:

- WRENA/ goes low and is inverted at gate B3-3
- IWON/ remains high and is inverted at gate B4-4
- IWON/ is again inverted at gate B3-11

- The two high outputs are ANDed at gate B4-5
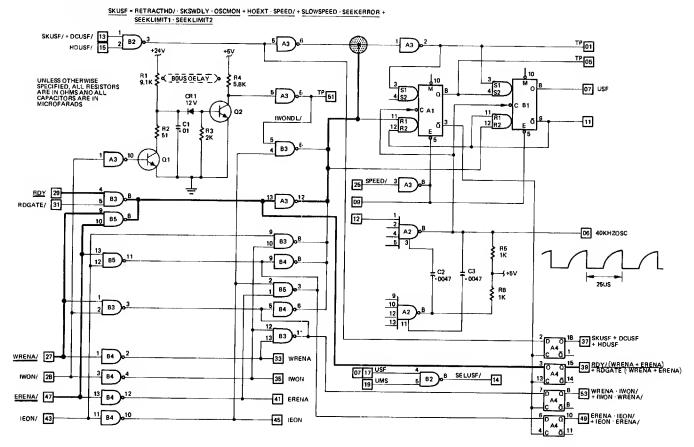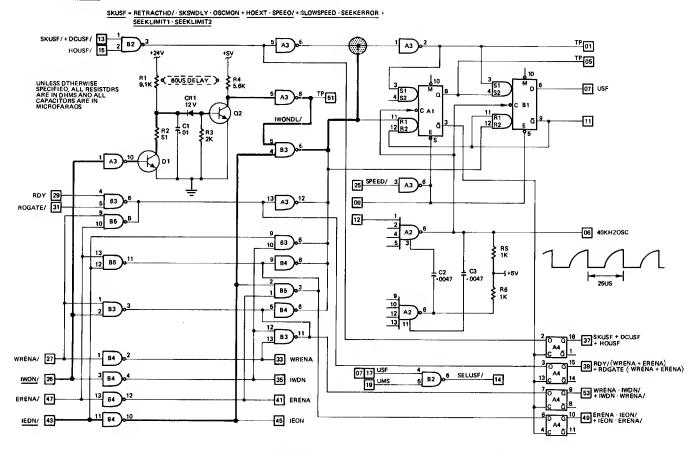- The collector ORed point goes low and the
  condition is latched as described in the Latching
  Unsafe Conditions paragraph

Figure 3-110. Unsafe Condition 10 (WRENA · IWON/)

$$U5F = \underline{5KUSF} + \underline{DCUSF} + \underline{HDUSF} + \underline{RDY}/(WRENA + ERENA) + \underline{RDGATE}\,(WRENA + ERENA) +$$
$$\underline{IWON}/\cdot IEON + \underline{IEDN}/\cdot IWON + \underline{ERENA \cdot IEON}/ + \underline{IEON \cdot ERENA}/ + \underline{WRENA \cdot IWON}/ + \underline{IWON \cdot WRENA}/$$

$$SKUSF = \underline{RETRACTHD}/\cdot SKSWDLY \cdot OSCMDN + \underline{HDEXT \cdot SPEED}/ + \underline{SLOWSPEED \cdot SEEKERROR} +$$
$$\overline{SEEKLIMIT1 \cdot SEEKLIMIT2}$$

UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS ARE IN MICROFARADS

If write current is detected (IWON) and WRENA/ is low (write enable not active), the following occurs:

- IWON/ goes low and is inverted at gate B3-3
- IWON/ is again inverted at gate B3-11

- WRENA/ remains high and is inverted at gate B4-2
- The two high outputs are ANDed at gate B4-6
- The collector ORed point goes low and the condition is latched as described in the Latching Unsafe Conditions paragraph

Figure 3-111. Unsafe Condition 11 (IWON · WRENA/)

PROGRAM SEEK ERRORS

During a program seek, two error conditions are monitored by the error detection logic: an attempt to seek to an illegal cylinder address and taking more than one second to achieve detent. These conditions are not latched by the unsafe latches and do not cause the SELECT LOCK indicator to light unless a first seek or restore is taking place. They do, however, cause seek incomplete (CSIN/;D) status to the controller.

Illegal Cylinder

During a program seek operation the cylinder address register is loaded. Logic is provided (Figure 3-112) to monitor illegal cylinder address combinations of 203 or above.
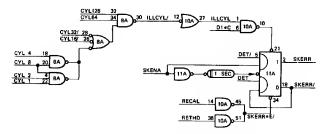
Figure 3-112. Program Seek Error Logic

If an illegal cylinder is detected, and the carriage traverses one cylinder position, the SKERR flip-flop is marked, and the positioning system goes into a non-detent non-velocity drift mode. It is then the task of the controller to interrogate the disk drive output lines

and find the cause of the problem. The controller can only clear a seek incomplete by a restore operation not by issuing another seek command.

More Than One Second to Detent

The set inputs to the SKERR flip-flop (Figure 3-112) are connected to DET/ and SKENA. During a program seek, SKERR is clocked one second after SKENA is set. If the detent flip-flop is not set prior to the clock pulse, SKERR sets. SKERR is ANDed with UNTSEL on the output interface logic and causes CSIN/;D (seek incomplete) low to the controller; as in an illegal cylinder condition, the controller can only clear a seek incomplete by a restore operation, not by issuing another seek command.

COMMUNICATIONS

When the controller communicates with a disk drive, it presents data to all drives simultaneously. However, an address selection/comparison scheme allows only the correctly addressed drive to accept and respond to the controller information.

Communications between the controller and disk drive takes place on two cables: Signal cable and DC cable. A signal cable is connected from the controller to the first drive in the system. The signal cable for each remaining drive is connected between drives as shown in Figure 3-113.
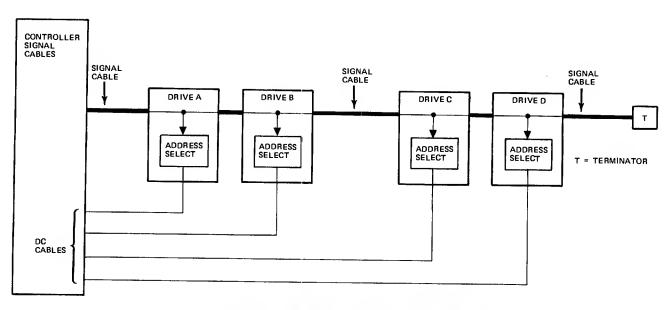
Figure 3-113. Signal Cable and Dc Cable Connections

From Figure 3-113, it can be seen that the connection between each drive and the connection to address select logic allows signal cable information to be bussed to all drives in a series-parallel fashion. The signal cable carries disk drive address lines, unit bus lines, tag lines and status lines.

A separate DC cable is connected from the controller to each drive. Each DC cable carries an acknowledgement signal that indicates, to the controller, that a specific drive has been addressed and selected. In addition, the DC cable provides a bi-directional read/write line.

The signal cable (Figure 3-114) contains eight bus lines (UB0/ - UB7/), nine address lines (UMS0/ - UMS7/, UMSSM/), and several status lines.

To start communications, the controller presents, to all drives in the system, a specific drive address on the address select lines. That is, the controller drops one of the UMS0/ - UMS7/, UMSSM lines. If the select logic address agrees with the address on the lines, the input
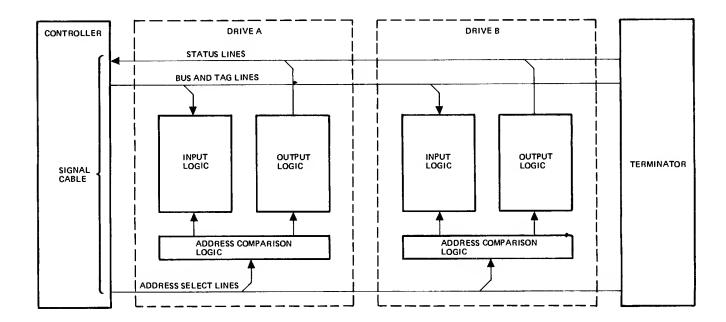
Figure 3-114. Signal Cable Connections

and output interfaces are enabled for that drive. The selected drive then sends, simultaneously, it's status on the status lines and a module selected acknowledgement signal (CMS/) on the DC cable (Figure 3-115).

The act of the drive being selected, and replying with module select (CMS/), logically connects the drive to the controller. Depending on the status, the controller then provides bus and tag information, to all drives in the system and only the logically connected drive responds.
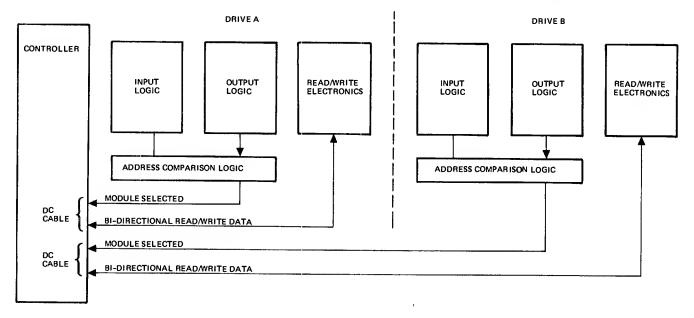
Figure 3-115. Dc Cable Connections

ADDRESS SELECTION

The controller begins communication with a disk drive by activating one of nine module select lines. The lines are named UMS0/ through UMS7/ and UMSSM/, representing logical modules zero through seven and the spare module.

Supplied with each disk drive are nine ID plugs, any one of which can fit in a recess in the operators panel of any drive. Each plug is unique in that it has a digit 0 through 7 or letter S on the front, and a corresponding post on the side of the plug (see Figure 3-116).

When inserting the ID plug into the drive, it is pushed in part way and then rotated until the post on the side of the plug lines up with the slot in the side of the plug hole. Rotating the plug causes a rotary switch (S10) to rotate and gate the correct module select line to the line receiver in the drive.
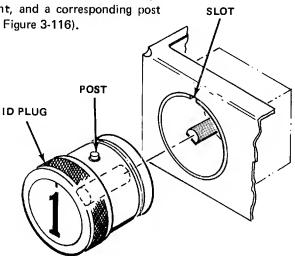
Figure 3-116. ID Plug

The drive logic is designed to prevent communication if an ID plug is not inserted in the drive. The drive detects the presence of an ID plug with a micro switch mounted behind the operator control panel.

INPUT INTERFACE

The input interface (Figure 3-117) comprises one pole of the nine select switches, the input line receivers, and the unit bus/tag interpretation logic.
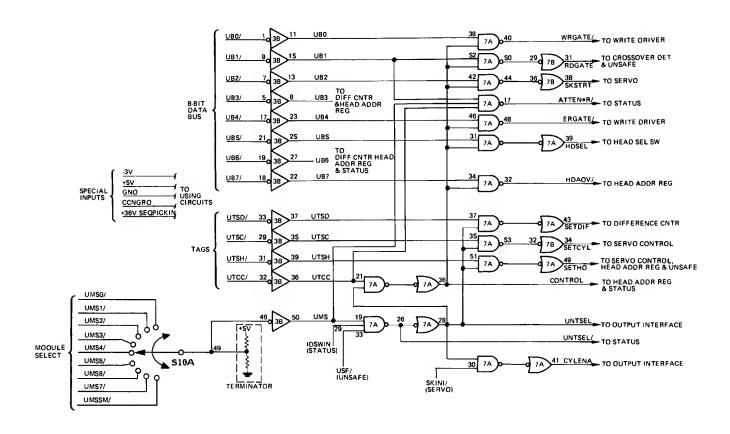
Figure 3-117. Input Interface Logic

When communications are to take place, the drive is selected and the interface enabled through one select switch pole by the module select line for that drive. The unit bus lines (UB0/ - UB7/) contain the information being transferred from the controller. The controller defines the information on the bus lines by activating one of four tag lines:

- UTSC — set cylinder
- UTSH — set head
- UTSD — set difference
- UTCC — control

The functions of the bus lines when defined by the four tags are shown in Table 3-1.

Figure 3-118 shows the bus line/tag timing. It should be noted that the timing shown applies to seek type operations only and not read or write operations. The unit bus lines remain active for the entire read or write operation. That is, the drive does not latch up read or write commands as it does seek type commands.

Table 3-1. Bus Line/Tag Line Definitions

Unit Bus Lines	Set Cylinder (UTSC)	Set Head (UTSH)	Set Difference (UTSD)	Control (UTCC)
UB0	Cylinder 128	Seek in Forward Direction	Difference 128	Write Gate (Active during entire write operation)
UB1	Cylinder 64	Reset Select Lock using Index	Difference 64	Read Gate (Active during entire read operation)
UB2	Cylinder 32	Not Used	Difference 32	Seek Start (Active for at least 800 nsec)
UB3	Cylinder 16	Head Address Register 16	Difference 16	Reset Head Address Register (Active for at least 800 nsec)
UB4	Cylinder 8	Head Address Register B	Difference 8	Erase Gate (Active during entire write operation +20 μsec
UB5	Cylinder 4	Head Address Register 4	Difference 4	Head Select (Active during entire read or write operation)
UB6	Cylinder 2	Head Address Register 2	Difference 2	Restore (Active for 15 to 20 msec)
UB7	Cylinder 1	Head Address Register 1	Difference 1	Head Advance (Active for at least 800 nsec)

Figure 3-118. Bus Line/Tag Timing

Input Interface Enable

If the drive is safe (USF/ high) and the ID plug is in (IDSWIN high) and the drive is selected (UMS high) a term is developed, UNTSEL (unit select high) which enables the input and output interface logic.

Tag Line Description

The following is a definition of each tag and a description of the associated unit bus line functions.

UTSH   Set Tag
         SETHD = UTSH · UNTSEL
Active after UB3 — UB7 is applied to the data bus, UTSH identifies the bus information as a 5-bit head address and a seek direction bit (UB0). (UB0/low=FWD)

UTSD   Set Difference Tag
         SETDIF = UTSD · UNTSEL
Active after UB0 — UB7 is applied to the data bus, UTSD identifies the bus information as an 8-bit cylinder difference count. The input is applied in 1's complement form of the difference between present and next selected cylinder addresses.

The most significant bit is UB0 and the least significant bit is UB7.

UTSC   Set Cylinder Tag
         SETCYL = UTSC · UNTSEL
Active after UB0 — UB7 is applied to data bus, UTSC identifies the bus information as an 8-bit cylinder address to be clocked into the cylinder address register.

The most significant bit is UB0 and the least significant bit is UB7.

UTCC   Control Tag
            Control = UTCC · UNTSEL
A control tag applied to the data bus, identifies information on the data bus as a control command. Each command is defined as follows:

Reset Head Address Register
UB3 · CONTRL
Clears the head address register

Seek Start
SKSRT = UB2 · CONTRL
Initiates a program seek

Read Gate
RDGATE = UB1 · CONTRL
Enables read circuits

Write Gate
WRGATE/ = UB0 · CONTRL
Enables write circuits

Erase Gate
ERGATE/ = UB4 · CONTRL
Enables erase current

Head Select
HDSEL = UB5 · CONTRL
Enables head selection

Restore
RESTORE/ = UB6 · CONTRL
Restores head carriage to cylinder 000 and resets head address register to 00

Head Advance
HDADV/ = UB7 · CONTRL
Increments the head address register one count

OUTPUT INTERFACE

Upon selection by the controller, the output interface will be enabled and status will be presented to the controller. Figure 3-119 shows the output interface logic.
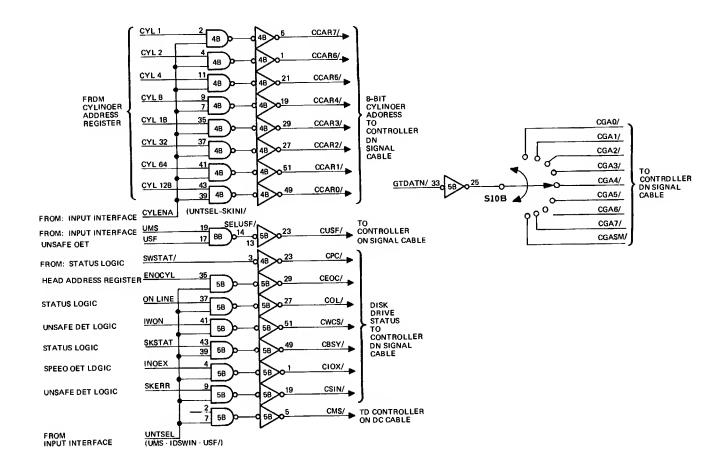
Figure 3-119. Output Interface Logic

STATUS

The logic signals which gate the status lines to the controller, are CYLENA for the Cylinder Address Register, UMS for Unsafe, and UNTSEL for the remaining status. CYLENA is equal to UNTSEL and not SKINI (first seek or restore). UNTSEL is equal to UMS, ID switch in, and not unsafe. Note that CGA0/ through CGA7/ and CGASM/ (Controller destined gated attention for modules 0 through 7 and spare module) are not gated by UMS. They are the controller interrupt lines which will be activated to notify the controller that the drive has finished a first seek, restore, or program seek operation.

Pack Change (CPC/)

The purpose of the pack change status line is to indicate, to the controller, that a disk pack may have been changed. The pack change status logic (Figure 3-120) includes the following major elements:

- ID Latch
- Change Detector Flip-Flop and Equality Gates
- Start Clock and Restore Clock
- Pack Change Latch
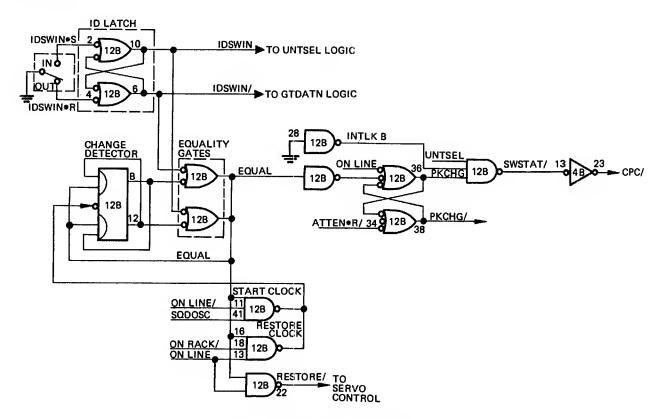
Figure 3-120. Pack Change Status Logic

ID Latch — The purpose of the ID latch is to copy the state of the ID switch. That is, detect the presence of the ID plug. If the ID plug is installed, the latch sets if the ID plug is removed, the latch resets.

Change Detector and Equality Gates — The purpose of the Change Detector and Equality gates are to produce a pulse called EQUAL each time the ID latch and the change detector are in the same state.

Start Clock and Restore Clock — The Start Clock and Restore Clock are used to toggle the change detector. Start Clock is used when the heads are retracted (ONLINE/high) and Restore Clock is used when the heads are extended (ONLINE/low).

Pack Change Latch — The Pack Change Latch (PKCHG) will set upon power application or if EQUAL goes high and will reset upon receipt of ATTEN * R/from the controller.

To describe the functions of the pack change status logic, the following conditions must be considered:

- Power On
- Off line (heads retracted) ID Plug Change
- On line (heads extended) ID Plug Change

Power On — Upon power application PWRINI/ erases the ONLINE flip-flop and ONLINE low sets the pack change latch. Upon the drive being selected, pack change status (CPC/) is sent to the controller.

Off Line ID Plug Change — If the ID plug is removed, the following occurs:

- ID latch resets
- EQUAL goes high because change detector and latch are in same state
- EQUAL high sets the pack change latch (PKCHG).
- At next SQDOSC, Start Clock (ONLINE/·SQDOSC) toggles change detector, causing EQUAL to drop
- Change Detector is now in next state of ID Latch

When the ID plug is installed the same events occur, except the ID latch sets.

On Line ID Plug Change — If the drive is on line (heads extended) and the plug is removed the following occurs:

- EQUAL goes high and sets PKCHG
- EQUAL·ONLINE produce RESTORE/ low
- RESTORE/ low causes a restore operation to occur

During the restore operation the slow flip-flop is set, which in turn erases ON RACK. ON RACK/ high and ONLINE produce a Restore Clock to toggle the change detector to the next possible state of the ID latch.

If the ID plug is installed, the same events occur and the next time the drive is selected, pack change status will be presented to the controller.

When the controller has checked the status lines from the drive, it will activate UTCC·UB1·UMS which will erase the attention flip-flop and reset PKCHG. PKCHG is reset to prevent the controller from interpreting the CPC status as another pack change at a later time.

From this description the following logical implications should be noted:

- A pack change will be indicated upon power up. The physical disk pack does not have to be changed
- A pack change will be indicated if the same ID plug is removed and reinstalled. The ID plug does not have to be changed
- If the heads are extended and the ID plug is removed or installed a restore operation will occur

Busy (CBSY)

CBSY/ is presented to the controller upon drive selection if the drive is performing a first seek, restore, program seek, or does not have the HDEXT (heads extended) latch set. The actual logical signal which monitors these conditions is Seek Ready (SKRDY). Obtaining a seek error (SKERR) will present not Busy Status by forcing SKRDY active (see Figure 3-121).

Figure 3-121. Busy Status Logic

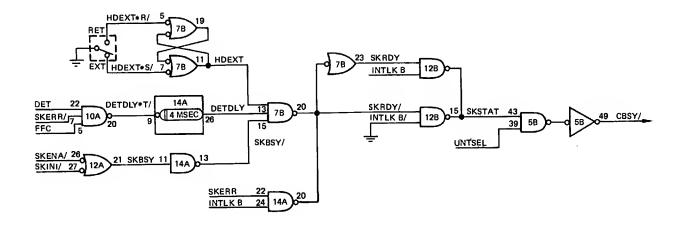During a first seek or restore operation, the seek initial flip-flop (SKINI) is marked as the operation begins, generating the line SKBSY. SKBSY is inverted and inhibits the SKRDY gate.

During a program seek operation, the seek enable flip-flop (SKENA) is marked as the operation begins, resulting in the same sequence of events as a first seek or restore.

At the end of a first seek, restore, or program seek, SKINI and SKENA are both off but the drive is not truly "ready" because of head and servo settling. Therefore, SKRDY is prevented for an additional period of time by detent delay (DETDLY), which is essentially FFC (flip-flop C in the Difference Clock Discriminator) delayed by four milliseconds.

The heads extended (HDEXT) latch directly reflects the position of the heads, i.e., loaded or unloaded. If the heads are in the retracted position, the heads extended/retracted switch resets the HDEXT latch, negating the SKRDY NAND.

SKRDY controls the state of SKSTAT: if SKRDY is high, SKSTAT is low, and vice versa. SKSTAT controls CBSY/; if SKSTAT is high, CBSY/ is low and vice versa. When the controller sees CBSY/ status, the disk drive is in detent mode and ready for further operations.

The following logic implications should be noted:

- A SKERR condition forces not Busy (overrides other conditions)
- Not heads extended produces Busy or
- DETDLY produces Busy; or
- SKENA or SKINI produces Busy
- Busy Status is not latched
- CBSY/ status is presented on the signal cable

Cylinder Address Register (CCAR0/-7/)

When the controller selects the disk drive, in preparation for a seek command, there are eight status lines which it must monitor: CCAR0 through CCAR7 (Controller destined Cylinder Address Register positions 0 through 7). CCAR0 is the most significant bit with a value of 128, and CCAR7 is the least significant with a value of 1. The controller must monitor these lines because they reflect the current position of the carriage; in order to compute the difference and direction between the current and new CAR values, the current cylinder address must be available.

In Figure 3-122, it can be seen that the combination of UMS, IDSWIN, not USF and not SKINI will activate CYLENA. CYLENA simply gates the value of the cylinder address register to interface drivers feeding the signal cable, and therefore to the controller.
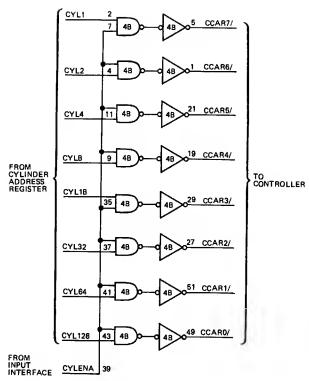
Figure 3-122. CAR Status Logic

End of Cylinder (CEOC/)

CEOC/, end of cylinder status is sent to the controller when the head address register (HAR) contains a value of 20 through 31. The valid heads are numbered 0 through 19: therefore 20 through 31 (31 is the maximum count in a five-bit register) truly at the "end of the cylinder".

This status line is present to prevent a possible unsafe condition from occurring: if a value of 20 through 31 is in the HAR, and Head Select is activated (UMS·UTCC·UB5), an unsafe condition (SELECT LOCK) occurs. However, if the controller first examines CEOC/ before selecting a head, a possible error condition is eliminated.

The End of Cylinder logic (Figure 3-123) monitors HAR bits 16, 8, and 4, in the following manner: if HAR16 and either HAR8 or HAR4 are on together, ENDCYL is active. This will present CEOC/ to the controller on the signal cable if UNTSEL is active.
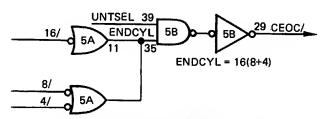

Figure 3-123. End of Cylinder Status Logic

Online (COL/)

COL/ (on line) status is presented to the controller when UNTSEL is active and the ONLINE flip-flop is set.

COL/ will be examined by the controller to determine if the heads are extended and the logic is not attempting to retract the heads (ACCOL inactive).

The ONLINE flip-flop (Figure 3-124) is set on a first seek by SKRDY, and remains set until either the heads are retracted (not HDEXT) or the logic is attempting to retract the heads (RETHD active). If ACCOL does go inactive, the next SODOSC resets the ONLINE flip-flop.
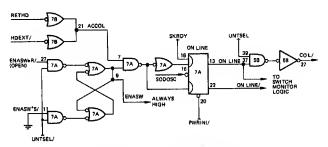
Figure 3-124. On Line Status Logic

Write Current Sense (CWCS/)

CWCS/ (Write Current Sense Status) is active from the selected drive whenever write current is flowing in a read/write head. This status is sent to the controller so it may verify that the data being sent to the drive on the read/write data coaxial line in the DC cable is being written.

When write current is being drawn by a selected head, the current flow through a resistance will cause a transistor to conduct, which will activate IWON/. IWON/ and UNTSEL will cause CWCS/ to go low. Figure 3-125 shows the write current sense logic.
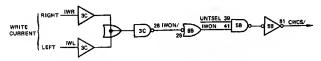
Figure 3-125. Write Current Sense Status Logic

- When write current is flowing through a read/write head, write current (IWON/) is low
- UNTSEL and IWON activate CWCS/ on the signal cable

Index (CIDX/)

CIDX/ (index status) occurs once per disk pack revolution on the selected drive. The controller uses CIDX/ status for synchronization of data transfer: all tracks begin at index.

The CIDX/ logic (Figure 3-126) comprises a NAND gate and an interface driver. UNTSEL is the enable line.
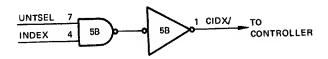
Figure 3-126. Index Status Logic

Seek Incomplete (CSIN/)

CSIN/ (seek incomplete status) is a program seek type error when presented as status, because if a seek incomplete occurs on a first seek or restore it results in an emergency retract.

Seek incomplete status is presented by the selected drive when the Seek Error (SKERR) flip-flop is on, and is an indication that the drive is in drift mode (not SKENA and not DET). The controller's reaction to CSIN/ should be a RESTORE command to erase SKERR and recover, if possible.

Figure 3-127 shows the Status logic for CSIN/.
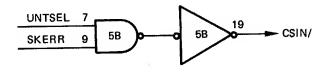
Figure 3-127. Seek Incomplete Status Logic

Module Selected (CMS/)

CMS/ is the only status which is presented on the DC cable. It is active when the drive is selected and provides the controller with a line from each disk drive which can be monitored for multiple drives selected (more than one CMS/ active), or to verify the selection of a drive, or to determine the physical (as opposed to logical) address of the selected drive.

The logic for Module Selected comprises an inverter and an interface driver, as shown in Figure 3-128, and is activated by UNTSEL.
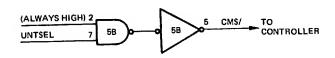
Figure 3-128. Module Selected Status Logic

Unsafe (CUSF/)

CUSF/ is active to the controller when the unsafe flip flops are set, and is gated by UMS.

Figure 3-129 shows the logic for Unsafe Status presentation.
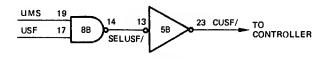
Figure 3-129. Unsafe Status Logic

Gated Attention (CGA0-7/ & CGASM/)

CGA0/ through CGA7/ and CGASM/ become active upon successful or error completion of a first seek, restore, program seek, or ID plug change. It is an interrupt condition independent of selection by the controller, and will cause the controller to interrogate the ending status of the first seek, restore, program seek, or ID plug change.

The controller can determine what type of operation caused the Gated Attention by selecting the drive and examining status. The following status combinations will be interpreted as shown:

- CGA(0-7 or SM)/ and CPC/ — first seek, restore, or ID plug change
- CGA(0-7 or SM)/ and not CPC/ — program seek
- CGA(0-7 or SM)/, CPC/, CSIN/, not CBSY/ and COL/ on or off — a seek error occurred after a first seek, restore, or ID plug change was initiated
- CGA(0-7 or SM)/, not CPC/, CSIN/, not CBSY/ and COL/ on or off — a seek error occurred after a program seek was started
- CGA(0-7 or SM)/, not CPC/, not COL/, CBSY/ and CSIN/ on or off — on a program seek, the heads were retracted or a seek logic problem occurred
- CGA(0-7 or SM)/, not CPC/, not COL/, not CBSY/, and CSIN/ on or off — on a program seek, RETHD became active.

Gated attention is generated in a slightly different manner for each condition which can cause it. Figure 3-130 shows the gated attention logic.

GTDATN/ = IDSWIN · (SKRDY+ACCOL/+SKERR) · SKSTRT/· ATTEN

ATTEN = ON LINE · VSLOW LATCH + SKSTRT
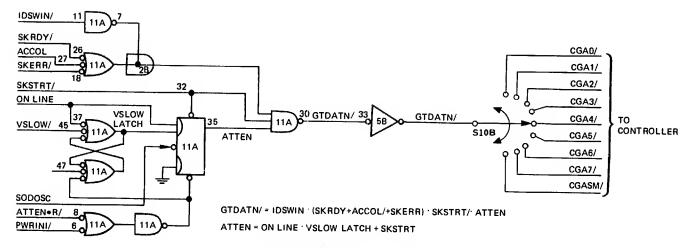
Figure 3-130. Gated Attention Status Logic

First Seek Gated Attention — During a First Seek, VSLOW/ is low and sets VSLOW LATCH. At the end of the First Seek, SKRDY/ and SKRDY occur; SKRDY/ and IDSWIN/ low cause the top leg of the GTDATN NAND to be high, while SKRDY, ACCOL, and SODOSC set ONLINE. ONLINE, VSLOW LATCH, and SODOSC set the ATTEN flip-flop, causing the bottom leg of the GTDATN NAND to be high, thus producing GTDATN/, since SKSTART/ is high.

Restore Gated Attention (Includes ID Plug Change) — Same as a First Seek Gated Attention except that the ONLINE flip-flop is already set, so the ATTEN flip-flop sets when the VSLOW LATCH sets. GTDATN/ is activated when SKRDY/ goes low.

Program Seek Gated Attention — The SKSTART/ pulse (CONTRL·UB2) from the controller that starts the program seek operation also marks the ATTEN flip-flop; thus, Gated Attention will occur at SKRDY/ time.

Seek Error Gated Attention — A Seek Error on a first seek, restore, or program seek will cause a gated attention by activating the same OR circuit that SKRDY/ activates. The ATTEN flip-flop is set as normal.

Loss of Access Online Gated Attention — Losing ACCOL during a first seek, restore, or program seek will cause a Gated Attention via the same OR circuit as SKRDY/ and SKERR/. The ATTEN flip-flop is set as it normally is.

When GTDATN/ goes active because of any of the previous conditions, an interface driver will transmit the Gated Attention to the controller on one of nine lines, CGA0/ through CGA7/ or CGASM/, depending on which ID plug is inserted in the operator's control panel. This will present the Gated Attention on the line corresponding to the logical address of the drive.

TYPICAL COMMUNICATIONS SEQUENCES

The following are two typical sequences, as examples of use, of the communication lines between a drive and its controller.

Program Seek and Write

During a normal program seek followed by a read or write operation the controller initiates the seek, then ceases communication with the drive. It is then up to the drive to cause a gated attention interrupt at the end of the seek, causing the controller to examine ending status and then proceed with the read or write operation.

Figure 3-131 is a timing diagram of a program seek followed by a write operation, with the significant events as follows:
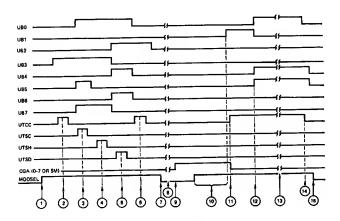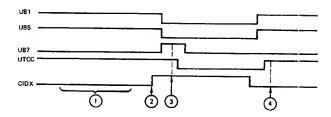
Figure 3-131. Seek and Write Timing Diagram

① Module select (UMS) is activated, selected drive presents status; controller examines status, decides it is satisfactory.

② UB3 and control tag reset the head address register prior to loading in a value. Reset HAR must precede set head tag.

③ UB0, 3, 5, 7, and set cylinder tag set the new cylinder position (149) in the CAR, erases SKFWD flip-flop, and marks 255 into the difference counter. Set cylinder tag must precede set head tag (set direction) and set difference tag (erase applicable position in difference counter).

④ UB0, 3, 7 and set head tag set SKFWD (UB0·UTSH) and enter 17 in the HAR.

⑤ UB0, 2, 4, 6 and set difference tag erase positions 128, 32, 8 and 2 from the difference counter, leaving 85. It can now be determined by deduction that at initial module select time, the controller received a value of 64 on the CAR status lines. (Forward 85 cylinders to cylinder 149 = 64, old CAR).

⑥ UB2 and control tag initiate the seek operation.

⑦ The controller drops module select, since disk drive communications is no longer required.

⑧ Access in motion during Seek (approximately 30 milliseconds).

⑨ Drive has finished seek and presents gated attention.

⑩ Controller activates module select, and examines status at end of seek.

⑪ UB1 and control tag erase the ATTEN flip-flop, turning off Gated Attention.

⑫ UB0, 4, 5 and control tag = Write, Erase and Head Select. The controller is now sending data on the read/write coaxial line in the DC cable.

⑬ Controller continues writing.

⑭ Controller ends write operation.

⑮ Controller drops module select, drive removes status from signal cable; operation terminated.

Head Advance and Read

A normally used tag sequence when searching for a particular section of information is: read, head advance, read, head advance, etc., until the information is found or the end of the cylinder is reached. Head advance increases the value in the HAR by one. The following timing diagram (Figure 3-132) shows a read in two successive tracks.

(1) A read operation (UB1, 5 and UTCC = read and head select) is taking place on a particular head.

(2) Index status is received by the controller.

(3) Controller drops read head select and raises head advance. The value in the HAR increases by one.

(4) Index status has fallen, and the controller begins a read and head select on the new track.

Figure 3-132. Head Advance and Read Timing Diagram

OEM OPTIONS AND DIFFERENCES

This section is divided into two major areas: OEM options and OEM differences. The following is a list of OEM options:

- Sector Generator — used for fixed length formats
- Subtractor — used when controller does not calculate cylinder address difference

OEM OPTIONS

Sector Generator Option

For fixed length recording formats, each disk surface can be divided into equally spaced, pie-shaped areas (sectors). The bottom disk of a sector-oriented disk pack (sector/index disk) contains a number of equally spaced sector notches and one index notch immediately after a sector notch. The sector generator logic, in conjunction with the index and speed detection logic, provides all, one-half odd, one-half even, or one-fourth of the sectors per disk revolution.

Sector/Index and speed Detection — The sector/index and speed detection logic (Figure 3-133) comprises an index/sector disk, a transducer, an operational amplifier functioning as a threshold detector, logic gates, three one-shots, a flip-flop, a relay driver, and sector generator logic.

The task of the sector/index and speed detection logic is to:

- Monitor index and sector pulses developed by the rotating sector/index disk, transducer, and threshold detector

- Provide index pulses to error detection logic and output status logic

- Provide sector pulses to the controller

- Determine when disk pack rotation achieves 70 percent of normal operating speed
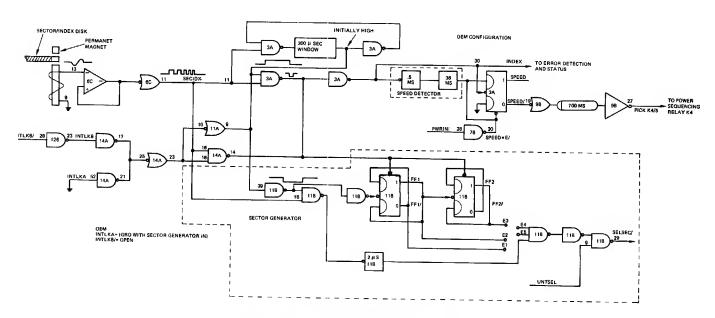
Figure 3-133. Sector/Index and Speed Detection Logic

The operating disk drive utilizes an interchangeable disk pack (Figure 3-134). The bottom disk of the pack contains a single index notch and a number of equally spaced sector notches, usually 20, machined into the disk edge.

Sector/Index Transducer — A transducer is used in conjunction with the sector/index disk. The transducer is fixed on a hinged assembly. The hinged assembly is mounted on the deck plate.

When the disk drive is operating, the transducer is positioned to enclose the edge of the rotating sector/index disk (Figure 3-134).
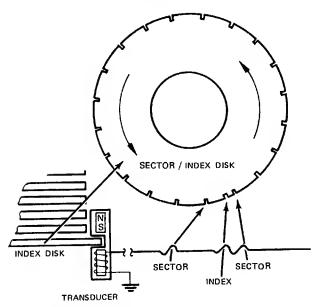
Figure 3-134. Sector/Index Disk and Transducer

As the disk pack rotates, the following occurs:

- The notches in the disk create an air gap during which the magnetic field from the transducer magnet is coupled to the transducer coil
- As the disk interrupts the magnetic field, there is minimum coupling
- As the disk rotates, the transducer develops pulses during each notch and a pulse train is provided to the sector/index and speed detection logic

Index Detection — The index detection logic (Figure 3-135) operates in conjunction with the index transducer and threshold detector. With each notched sensed, a positive-going index pulse (SECIDX) is produced. As the notched disk rotates, a pulse train comprised of index pulses and sector pulses is developed. The pulse train is applied to three 2-input NAND gates marked A, B, and C in Figure 3-135.

When a sector generator module is installed INTLKA (interlock A) is fixed at ground and NAND gate C is disabled. This provides an initially high input to gate D, which in turn allows firing the 300-microsecond one-shot window on the trailing edge of every sector pulse (NAND A). The purpose of the 300-microsecond window is to separate index pulses from sector pulses, allowing only index pulses to be applied to the speed detection logic.

Figure 3-135 shows a pulse train comprised of sector pulses and one index pulse.
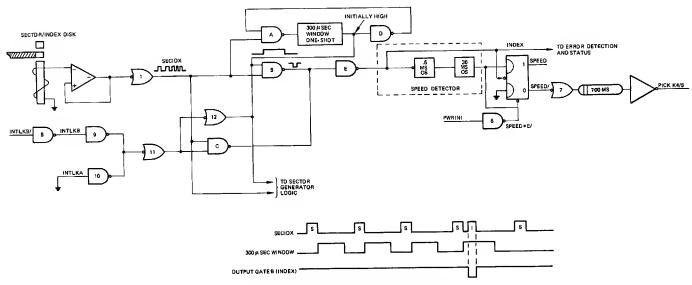
Figure 3-135. Index Detection, Sector Option

Since the 300-microsecond one-shot fires on the trailing edge of the sector pulse, the 300-microsecond one-shot output is low during the sector pulse inhibiting the sector pulses to the speed detection logic.

When the index pulse occurs, immediately following the last sector pulse, the 300-microsecond window is high, gating the index pulse to the speed detection logic via NAND B.

The pulse train is inverted by gate E and sent to error detection logic and output status logic. At controller interrogation time, the INDEX pulse train provides 50 microsecond CIDX/ timing pulses to the controller for data transfer synchronization.

Sector Detection — The purpose of the sector detection logic (Figure 3-136) is to separate the index pulses from the sector/index pulse train and to provide a clock, at sector time, to sector counter flip-flops FF1 and FF2.

As sector and index pulses are generated, 300-microsecond windows are also generated. Gate A inverts the window so that it is high at sector time and low at index time.

The input to gate B is the sector/index pulse train; however, only the sector pulses are enabled because gate A output is low at index time. The negative output of gate B, inverted sector pulses, are applied to a 2-microsecond one-shot which narrows the sector pulse width. The inverted window pulse output of gate A also clocks FF1, advancing the 2-stage counter each time a sector pulse occurs.
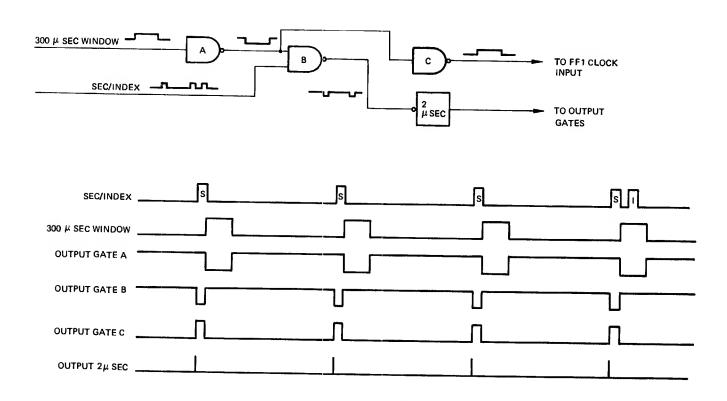
Figure 3-136. Sector Detection

Selected Sector Generation — The sector generator logic (Figure 3-137) provides the means of selecting a specific quantity of sectors per each disk revolution.

Both flip-flops are direct-reset at the negative transition of each index pulse (every disk revolution).

The output of the counter flip-flops can be connected to provide the following sector options:

- All
- One-half odd
- One-half even
- One-quarter

Flip-flops FF1 and FF2 comprise a 2-stage counter. FF1 is toggled by the trailing edge of the window pulse that occurs 300 μsec. after each sector pulse. FF2 is clocked by the negative transition of FF1 one-side output. Thus, FF1 changes state once per sector pulse, while FF2 changes state on alternate sector pulses.

The outputs of FF1 and FF2 can be connected to gate D, as shown in Table 3-2, to provide the following sector options.

Table 3-2. Sector Options

SECTOR OPTIONS	FROM	TO
All	Open	Open
½ odd	E1	E4
½ even	E2	E4
¼	E2	E4
	E3	E5

The first sector following the index pulse is sector one; the remaining sector are consecutively numbered.

- All sectors — no jumpers required,
- ½ odd — 1 odd numbered sector generated each time FF1 sets
- ½ even — 1 even numbered sector generated each time FF1 resets
- ¼ — 1 sector generated, each time FF1 and FF2 are both set
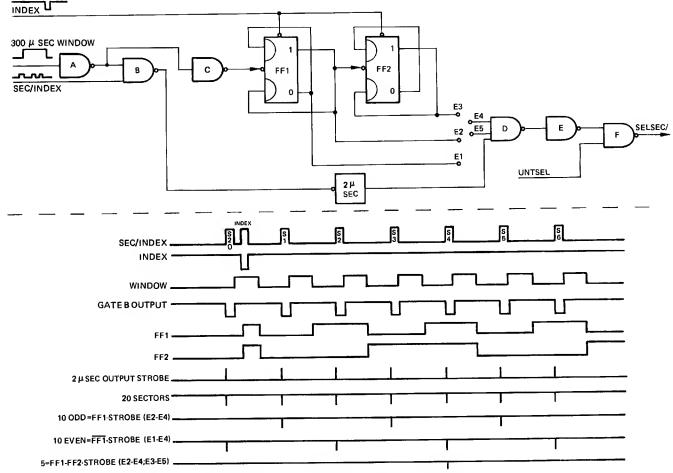
Figure 3-137. Sector Generation Logic, 20 Sector Pack

FF1 and FF2 are ANDed with a 2-microsecond single-shot at gate D. The 2-microsecond single-shot is generated at the positive transition of each sector pulse in the sector/index pulse train.

The output of gate D is a negative-going 2-microsecond pulse at the selected sector time. UNTSEL is ANDed at output gate F to produce SELSEC/ to the output interface logic. When SELSEC/ is low the output interface logic develops CSECT/ (controller destined SECTor).

Subtractor Option

The subtractor computes the difference between the present cylinder address and the desired cylinder address and supplies the difference to the difference counter. It is not necessary for the controller to read the present cylinder address and calculate the difference and direction as in the standard disk drive. With the subtractor option, the controller supplies only the desired cylinder address and the subtractor provides the difference and direction. Figure 3-138 is a simplified block diagram of the subtractor and associated logic. If the subtractor is not used a jumper board is installed and difference calculations are performed by the controller.
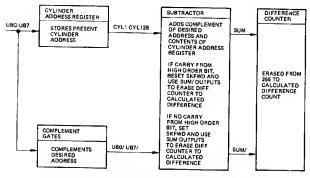

Figure 3-138. Subtractor, Simplified Block Diagram

- Cylinder Address Register — stores present cylinder address and is loaded at set cylinder tag time (SETCYL)
- Complement Gates — invert the states of UB0—UB7 (desired cylinder address from controller)

- Subtractor — essentially an 8-bit parallel adder with end-around-carry. Performs subtraction by summing complement of desired cylinder address with present cylinder address — gates the SUM or SUM/ outputs to the difference counter

- If a carry is propagated from the last bit (128), the following occurs:
  1. Add a carry into the low order bit
  2. The SUM/ of each stage is gated to the difference counter at the fall of SETCYL erasing the difference counter from 255 to the calculated difference
  3. The SKFWD flip-flop remains reset

- If there is no carry from the last stage, the following occurs:
  1. The SUM outputs are gated to the difference counter at the fall of SETCYL, erasing the difference counter from 255 to the calculated difference
  2. The SKFWD flip-flop is set

Subtractor Logic — The subtractor logic is shown in Figure 3-139.

- The gates preceeding each stage, complement the desired cylinder address (UB0 — UB7)
- The gates connected to the output of each stage gate either the SUM or SUM/ outputs to the difference counter, depending on whether a carry was propagated from the last stage (bit 128)

When the controller sends the desired cylinder address on UB0 — UB7, the following occurs:

- The complement gates invert the states of UB0 — UB7 and apply the complemented bus lines to the adder
- The present cylinder address is added to the complemented bus lines (UB0/ — UB7/)
- All carrys are propagated to the next higher order bit until there are no further carrys
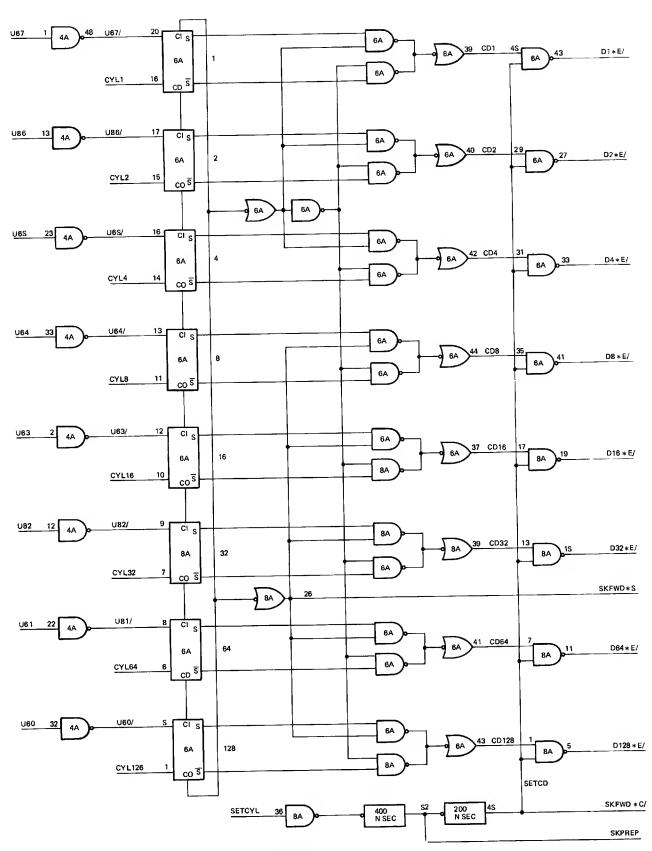
Figure 3-139. Subtractor Logic

Typical Adder Stage — Each adder stage sums three bits: A, B, and CI (carry in) from previous stage, and provides three outputs: SUM SUM/ and CO (carry out) to the next stage. Figure 3-140 shows a block diagram of an adder stage and a truth table for the variables in one stage.

- Column A represents variables UB0/ — UB7,
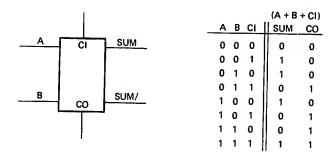- Column B represents variables CYL1 — CYL128,

Subtraction Process — To explain the subtraction process, two conditions are given:

- Present cylinder address greater than new cylinder address
- New cylinder address greater than present cylinder address

Table 3-3 is a truth table showing the subtraction process when the present cylinder address is 128 and the new cylinder address is 100

		(A + B + CI)	
A B CI		SUM	CO
0 0 0		0	0
0 0 1		1	0
0 1 0		1	0
0 1 1		0	1
1 0 0		1	0
1 0 1		0	1
1 1 0		0	1
1 1 1		1	1

Figure 3-140. Typical Adder Stage

Table 3-3. Present Cylinder Address Greater Than New Cylinder Address

1 NEW CYLINDER	2 NEW CYL/	3 PRESENT CYL	4 SUM	5 CARRY	6 CARRY$_1$	7 SUM$_1$	8 SUM$_1$/	9 SUM/·SET CD
U87=0	1	CYL1=0	1	0	1	0	1	0
UB6=0	1	CYL2=0	1	0	1	0	1	0
U85=1	0	CYL4=0	0	0	1	1	0	1
UB4=0	1	CYL8=0	1	0	LAST→0 CARRY	1	0	1
UB3=0	1	CYL16=0	1	0		1	0	1
UB2=1	0	CYL32=0	0	0		0	1	0
UB1=1	0	CYL64=0	0			0	1	0
UB0=0	1	CYL128=1	0	1→REV		0	1	0
100	127	128				28	227	28

- Column 1 — bit configuration of the new cylinder address
- Column 2 — complement of the new cylinder address
- Column 3 — present cylinder address
- Column 4 and 5 — sum and carry out from each stage of the subtractor. Notice that a carry out is propagated from bit 128 to leave the SKFWD flip-flop set
- Column 6 and 7 — end-around-carry (CARRY 1) and second sum (SUM$_1$), respectively
- Column 8 — complement of the sum
- Column 9 — result of ANDing SETCD with the complement of the sum; the final output to erase the difference counter to a count of 28

Table 3-4 is a truth table showing the subtraction process when the present cylinder address is 100 and the new cylinder address is 128.

Table 3-4. New Cylinder Address Greater Than Present Cylinder Address

1 NEW CYLINDER	2 NEW CYL/	3 PRESENT CYL	4 SUM	5 CARRY	6 SUM·SETCD
UB7=0	1	CYL1=0	1	0	0
UB6=0	1	CYL2=0	1	0	0
UB5=0	1	CYL4=1	0	1	1
UB4-0	1	CYL8=0	0	1	1
UB3=0	1	CYL16=0	0	1	1
UB2=0	1	CYL32=1	1	1	0
UB1=0	1	CYL64=1	1	1	0
UB0=1	0	CYL128=0	1	0 FWD (No Carry)	0
128	127	100	227		28

- Column 1 — bit configuration of the new cylinder address
- Column 2 — complement of the new cylinder address
- Column 3 — present cylinder address
- Column 4 and 5 — sum and carry of each stage. Notice that a carry is not propagated from bit 128, therefore the SKFWD flip-flop is set
- Column 6 — final output to the difference counter, which is the ANDing of SUM and SETCD. The difference counter is erased to a difference of 28

Subtractor Timing

The subtractor timing circuits and logic are shown in Figure 3-141.

SKPREP is used to develop D*M/;01, D*M/;02 and SKFWD*E to erase difference counter to 255 and the SKFWD flip-flop. SKPREP is developed 200 nanoseconds before SETCD. SKPREP marks the difference counter and erases SKFWD 200 nanoseconds before the difference counter is erased to the calculated difference, and the SKFWD flip-flop is clocked.

SETCD enables the SUM or SUM/ output to erase the difference counter to calculated difference and a carry sets SKFWD.
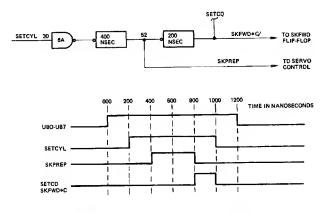

Figure 3-141. Subtractor, Timing Diagram

Interface Options

There are two interface options:

- ±3 volt O level
- +5 volt D level

Figure 3-142 shows the circuit configuration for each type of interface.

OEM DIFFERENCES

- Operator-controlled on-line logic
- Hardwired module select line (no ID plug)
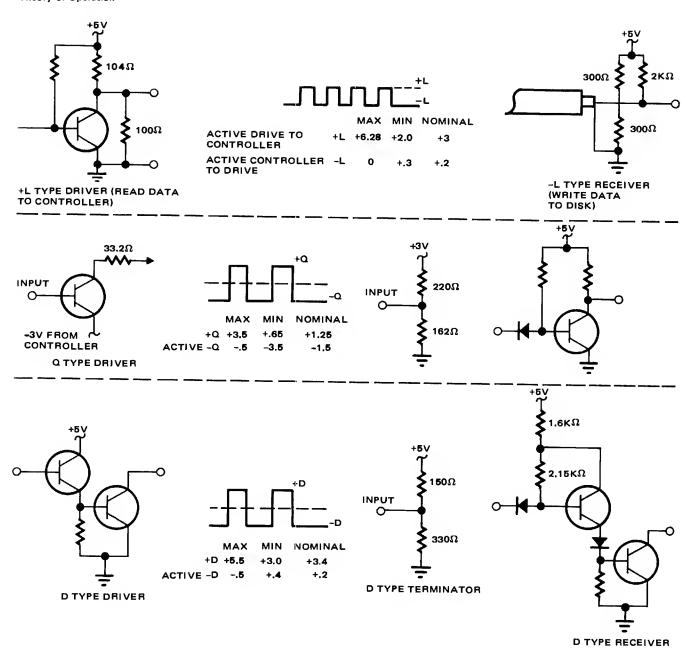- Seek Ready logic
- Initiating power-up sequence

+L TYPE DRIVER (READ DATA
TO CONTROLLER)

ACTIVE DRIVE TO CONTROLLER		MAX	MIN	NOMINAL
	+L	+6.28	+2.0	+3
ACTIVE CONTROLLER TO DRIVE	-L	0	+.3	+.2

-L TYPE RECEIVER
(WRITE DATA
TO DISK)

Q TYPE DRIVER

		MAX	MIN	NOMINAL
	+Q	+3.5	+.65	+1.25
ACTIVE	-Q	-.5	-3.5	-1.5

D TYPE DRIVER

		MAX	MIN	NOMINAL
	+D	+5.5	+3.0	+3.4
ACTIVE	-D	-.5	+.4	+.2

D TYPE TERMINATOR

D TYPE RECEIVER

Figure 3-142. Interface Options

Interlocks A and B

In the OEM drive INTLKA is connected to ground when the sector generator module is installed. INTLKB/ is open at all times and affects the on-line logic, read only logic and seek ready logic.

Read Only

The read only logic provides the means of manually inhibiting a write operation for data protection purposes.

The purpose of the read only logic (Figure 3-143) is to inhibit the WRGATE and ERGATE lines. The read only function can only be initiated prior to drive selection. Once the drive is selected, the state of the READ ONLY switch is logically disconnected from the read only logic.

The read only function is enabled by UNTSEL/ high. When the drive is selected, UNTSEL/ goes low and the RD ONLY latch cannot be altered by the READ ONLY switch. If the RD ONLY latch was previously set, writing is inhibited.
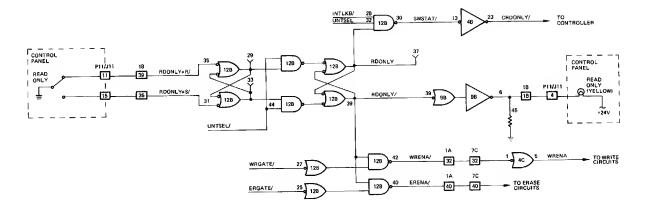
Figure 3-143. Read Only Logic

If the READ ONLY switch is actuated prior to drive selection the following occurs:

- RDONLY*R/ goes low and sets the first latch

- If the drive is not selected, the RDONLY latch sets

- RDONLY/ low causes WRENA/ high and ERENA/ high, to disable the write and erase circuits

- RDONLY/ low, lights the READ ONLY indicator

- RDONLY also develops CRDONLY/ status

On-Line

The on-line logic provides the means of manually controlling the on-line/off-line status of the drive prior to the drive being selected.

The purpose of the on-line logic (Figure 3-144) is to indicate to the controller, operator, and drive logic, when the disk drive is on line.

The on-line latch can only be set or reset prior to drive selection. UNTSEL/ high enables the latch prior to the drive being selected. When the drive is selected, UNTSEL/ goes low and the on-line switch has no affect on the latch.

If the device letter indicator/switch is actuated prior to drive selection, the following occurs:

- ENASW*R/ goes low and sets the on-line latch,
- When the heads are extended (ACCOL), the on-line flip-flop sets,
- The device letter indicator/switch lights if the following conditions are met:
  1. not restore,
  2. not seek error,
  3. positioning system on rack,
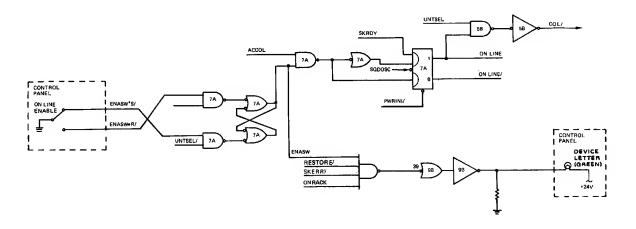- ON LINE high develops COL/ low to the controller.

Figure 3-144. On-Line Logic

Selecting Disk Drive

The OEM drive does not have provisions for selectable addressing. A unique line (UMS/) is connected via the dc cable from the controller to each drive in the system. A drive is selected when UMS/ is active.

Seek Ready Logic

In the OEM application, SKRDY is not forced active when a SKERR (Seek Error) occurs. This is because INTLKB is always low in the OEM version. See Figure 3-145.
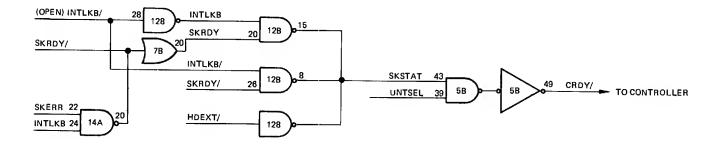

Figure 3-145. Ready Status Logic

Initiating Power-Up

To initiate a power-up sequence, the controller does not supply +36V SEQ PICKIN and CCNGRD. When AC POWER switch S1 is set to ON, the following occurs. Refer to Figure 3-146.

- +45 volts is developed and 9 volts is dropped across resistor R7,
- +36 volts is routed to the controller on J3-78,

- Controller returns +36 volts as +36V SEQ PICKIN on J3-77,

- Power sequencing begins as in standard drive,

- When K6 picks, +36V SEQ PICKOUT is routed to next drive in line.
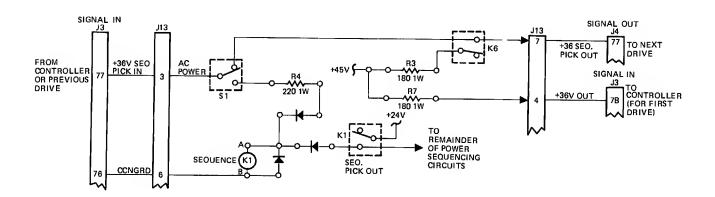

Figure 3-146. Power-Up Circuits

MODEL 114 CONFIGURATIONS

Table 3-5 is a list showing each current model configuration.

Table 3-5. Model 114 Disk Drive Configurations

| Type	Model	Line Freq (Hz)	Interface Level	Read/Write Data Level	Subtractor Supplied	Sector Generator Available
OEM	002	60	+5V DTL	+5V L	No	Yes
OEM	002	50	+5V DTL	+5V L	No	Yes
OEM	003	60	+5V DTL	+5V L	Yes	Yes
OEM	004	50	+5V DTL	+5V L	Yes	Yes
OEM	005		(reserved - this model not released)			
OEM	006	60	±3V Q	+5V L	No	Yes
OEM	007	50	±3V Q	+5V L	No	Yes
OEM	008		(reserved - this model not released)			
Std	009	60	+5V DTL	+5V L	No	No
Std	010	50	+5V DTL	+5V L	No	No
Std	011	60	±3V Q	+5V L	No	No
Std	012	50	±3V Q	+5V L	No	No
Std	013	60	+5V DTL	+5V L	No	No
Std	014	50	+5V DTL	+5V L	No	No
Std	015	60	+5V DTL	+5V L	No	No
Std	016	50	+5V DTL	+5V L	No	No

SECTION 4
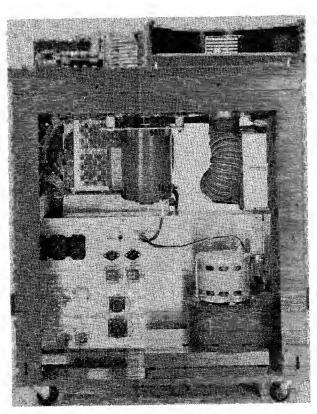
PREVENTIVE MAINTENANCE

GENERAL

The preventive maintenance required to ensure optimum performance of the disk drive is highly influenced by the environment conditions and the type of use that the unit is subjected to. Periodic checks, visual inspection and cleanliness are the basis for the following preventive maintenance procedures.

A preventive maintenance schedule is included to be utilized as a guide by the maintenance personnel involved in servicing the disk drive. Refer to Figure 4-1.

VISUAL INSPECTION

The first step in any preventive maintenance schedule is careful and thorough visual inspection for signs of dirt, wear, cracks, binds, loose connections, or loose hardware. Performing the preventive maintenance for any of these problems will greatly extend equipment life.

CLEANLINESS

The second step in preventive maintenance is cleanliness. A clean internal and external environment will enhance
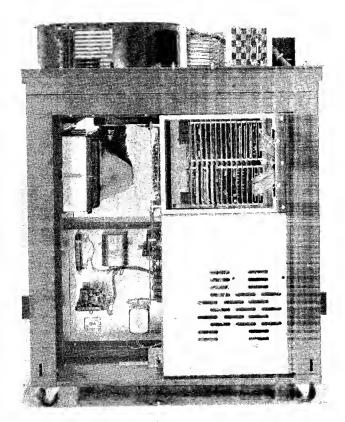

Figure 4-1. Model 114 Disk Drive — Front and Rear Views (Exposed)

equipment life and appearance. Dirt and grime not only look bad but also cause wear. An unclean disk drive is extremely detrimental to the read/write heads, the disk pack, and data storage capability.

The importance of visual inspection and cleanliness of the disk drive cannot be over-emphasized. Many

problems need never occur if cleanliness is observed.

It is recommended that maintenance personnel read each procedure thoroughly, prior to performing that procedure, and to perform grouped procedures concurrently.

PREVENTIVE MAINTENANCE SCHEDULE

MONTHLY PREVENTIVE MAINTENANCE PROCEDURES

The following tasks are to be accomplished monthly:

- Check the read/write heads; inspect, and if necessary, clean.
- Clean the disk pack area.
- Check the disk cleaning brushes.
- Change the input filter.
- Check the absolute air filter pressure.
- Check the spindle grounding brush.
- Clean the external surfaces of the disk drive.

Materials required to perform these tasks are:

- Freon TF
- Tongue depressors or cotton-tipped swabs (Q-tips)
- Inspection mirror — (dental)
- High intensity lamp (flashlight)
- Soft lint-free cloth (gauze)
- Commercial cleaner (soft detergent)
- Emery cloth (fine)
- Voltohmmeter (VOM)
- Air pressure gauge

NOTE

Most of these items may be purchased locally.

READ/WRITE HEADS

The following paragraphs define the types of contamination and head-to-disk interference that may occur to read/write heads.

During normal read/write operations the disk surfaces may become slightly scratched. This type of scratch would look similar to a "polishing" scratch and is insignificant as long as data can be properly recovered. However, there are types of head-to-disk interference that can cause significant damage to the disk pack and the read/write heads. Dirt and dust particles, oxide, and residue buildups on either the disk pack or the read/write heads, are some of the most common types of head-to-disk interference.

Dirt and dust particle damage occurs when a foreign particle becomes wedged between the "flying" read/write head and the spinning disk. The particle may become embedded in the disk surface or in the epoxy of the read/write head and is likely to leave a deep groove at the point of entry. If the particle remains embedded in the read/write head it will damage the disk and destroy not only that particular track but that entire disk surface. If the particle is not detected during preventive maintenance procedures the particle may eventually become dislodged and become wedged between another head and the disk pack.
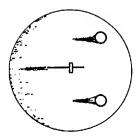
Oxide buildup may occur on the disk pack or the read/write heads. Oxide can be picked up by the read/write heads of dirty disk packs. When the accumulation of oxide exceeds a given point on the read/write heads it begins to rub on the disk surface accumulating more oxide. The result of the oxide accumulation is a useless read/write head and a damaged disk pack.

Residue buildup may also occur on the disk pack or the read/write heads. Residue buildup is usually the result of contaminates introduced onto the disk pack or read/write heads. These contaminates are usually alcohol residue left after cleaning either the disk pack or the read/write heads, fingerprints which contain oils and salts, or a contaminated environmental atmosphere such as smoke. The results of residue buildup, if not detected, are the same as particle and oxide buildup; a useless head or heads, and a damaged disk pack.
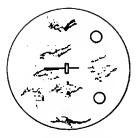
An early indication of these types of head-to-disk interference are an excessive number of intermittent read errors. Therefore, the importance of preventive maintenance cannot be overemphasized.

During the preventive maintenance procedures the read/write heads should be inspected for the following conditions (see Figure 4-2).
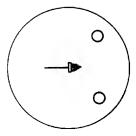
- Scratches and grooves
- Oxide buildup
- Residue Buildup
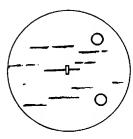- Fingerprints and other oil-like stains

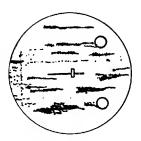A. Slight oxide buildup. Head should be cleaned and used.

B. Alcohol residue. Head must be cleaned.

C. Oxide buildup in pole piece. Head must be replaced.

D. Slight scratches. No oxide buildup. Head is usable.

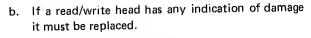E. Oxide buildup due to scratches. Head must be replaced.

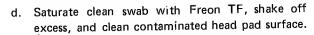F. Crashed (usually burned). Head must be replaced.

Figure 4-2. Read/Write Head Contaminates

```
CAUTION
```

Do not touch the head surfaces with the inspecting tools. Clean the heads ONLY if they are dirty.

a. Utilizing a light source and an inspection mirror, individually inspect each read/write head for any indication of damage or contamination (see Figure 4-3).

READ/WRITE HEADS

Figure 4-3. Read/Write Heads

b. If a read/write head has any indication of damage it must be replaced.

c. If a read/write head has any indication of contamination it must be cleaned.

d. Saturate clean swab with Freon TF, shake off excess, and clean contaminated head pad surface.

e. Using lint-free cloth, wipe head pad surface dry.

f. Reinspect head surface to ensure head is clean and there is no residue. Inspect surrounding heads to ensure they have not been contaminated by cleaning materials.

g. If any head is extremely dirty it may be necessary to remove head and clean it more thoroughly with alcohol. If so, perform read/write alignment procedures after replacing head.

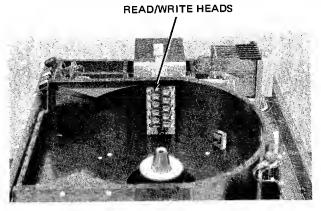h. After the heavy oxide has been removed, clean head with Freon TF to remove all residue.

DISK PACK AREA

a. Wipe inside of air shroud with lint-free cloth dampened with alcohol. Ensure that residue is removed (see Figure 4-4).
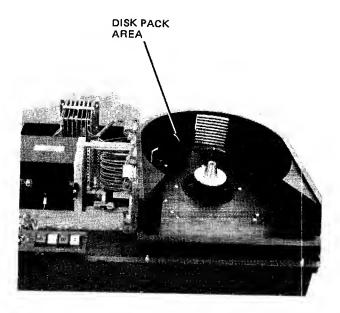
Figure 4-4. Disk Pack Area

b. Wipe inside of cover and ensure that residue is removed.

DISK CLEANING BRUSHES

a. Utilizing a light source, individually inspect each brush head for worn or contaminated brushes (see Figure 4-5).
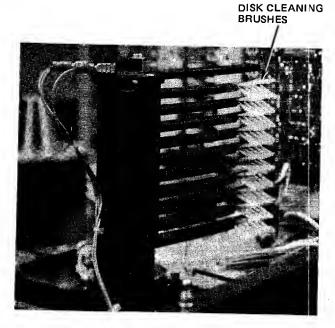

Figure 4-5. Disk Cleaning Brushes

b. If any brush head shows indication of worn or contaminated brushes replace the brush head.

c. Inspect each set of brushes on brush head for correct angularity (see Figure 4-6).
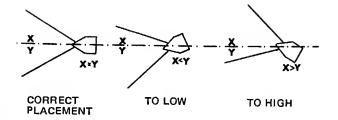

Figure 4-6. Brush Angularity Check

d. If brush angularity is incorrect replace brush head.

e. Prior to installing new brush head ensure that brush holder has no flashes or burrs where shoulder of brush head fits into brush holder (see Figure 4-7).
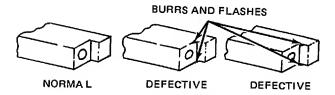

Figure 4-7. Brush Holder

INPUT AIR FILTER

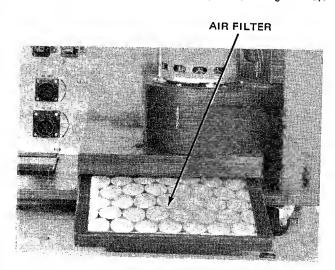a. Remove input air filter and replace (see Figure 4-8).

Figure 4-8. Input Air Filter Removal/Installation

b. If new filter is not readily available, clean existing filter by tapping one edge of the filter on a hard surface.

ABSOLUTE FILTER AIR PRESSURE

a. Utilizing portable air pressure gauge, measure air pressure on filter output plenum (see Figure 4-9).
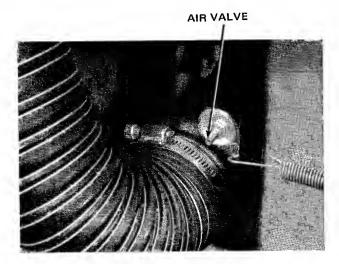
AIR VALVE

Figure 4-9. Air Pressure Check

b. Pressure must be positive; if not, replace filter.

SPINDLE GROUNDING BRUSH

a. With disk pack installed and disk drive powered-up utilize a voltohmmeter (VOM) and check for continuity from spindle shaft collar to deck plate assembly (see Figure 4-10).
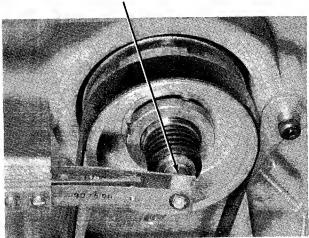
SPINDLE GROUNDING BRUSH

Figure 4-10. Spindle Grounding Brush

b. If continuity check indicates greater than 1 ohm resistance, insert piece of fine emery cloth between brush and brush contact. Slide emery cloth back and forth while disk is rotating.

c. Repeat continuity check.

d. Remove all emery cloth particles and dust from brush contacts.

EXTERNAL SURFACES

a. Clean external surfaces of disk drive with a soft cloth dampened with a commercial cleaner.

b. Ensure that residue is cleaned away.

SEMIANNUAL PREVENTIVE MAINTENANCE PROCEDURES

The following tasks are to be accomplished semiannually:

● Monthly Preventive Maintenance Procedures

● Clean the internal surfaces of the disk drive

● Change the absolute air filter

● Check the spindle system

● Check the positioning system

● Check the read/write system

Materials required to perform these tasks are:

● As specified for the monthly procedures

● Oscilloscope

● Disk Drive Exerciser — Models 2011, 2015 or Control Unit In-Line Diagnostics

● Sta-Lube Molybdenum grease

● Silicon-lube

INTERNAL CLEANLINESS

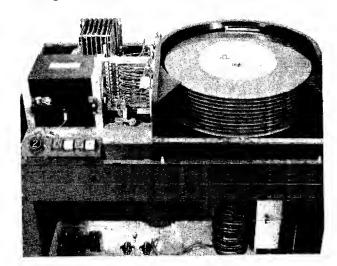a. Remove front and rear panels, and remove top right- and left-hand covers (see Figure 4-11).

Figure 4-11. Panels and Covers Removed

b. Inspect and remove any accumulation of dirt and dust.

SPINDLE SYSTEM

a. Remove disk pack.

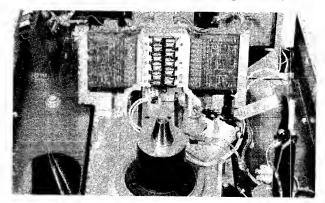b. Check spindle surface for dirt and wear. Clean spindle surface with alcohol (see Figure 4-12).

Figure 4-12. Exposed Deckplate W/O Shroud

c. Do not lubricate spindle cone surface.

d. With an alcohol-dampened swab, remove accumulated dirt, shavings, and grease from threaded hole in spindle.

e. After hole is thoroughly cleaned apply light coat of grease to threads.

f. Ensure that disk pack can be easily installed and removed.

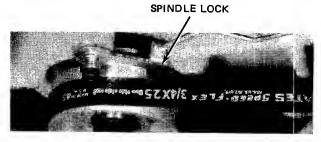g. Check spindle lock for freedom of movement and alignment (see Figure 4-13).

SPINDLE LOCK

Figure 4-13. Spindle Lock Check

h. Check pack switch for burned or dirty contacts. Clean contacts with fine emery cloth as required (see Figure 4-14).

i. If contacts are badly burned pack switch should be replaced.

j. Check spindle belt for frayed edges and alignment.

k. Check spindle belt tension.

l. Insert spring scale gauge in elongated hole on left side of motor mount (see Figure 4-15).
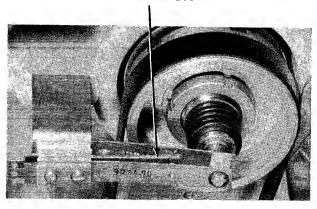
SWITCH CONTACTS

Figure 4-14. Pack Switch Contacts

ELONGATED HOLE
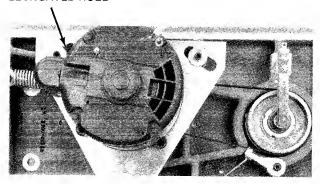
Figure 4-15. Drive Belt Tension Check

m. Pull gauge toward right, front cover of drive until motor moves. Pulling force required to move drive motor should be between 14 − 20 pounds. If force required is less than 14 pounds, replace drive belt.

n. Check sector/index transducer positioning.

o. Move transducer tilt bracket manually back and forth, to simulate opening and closing of disk pack access door.

p. Observe that transducer repositions properly. If not, remove air shroud, disassemble transducer positioning assembly, and apply light coating of Sta-Lube to entire pivoting shaft.

q. Reassemble transducer positioning assembly, recheck positioning, and ensure that tension spring is not too tight.

r. Install disk pack, place 0.033-inch feeler gauge between disk pack and sector/index transducer (see Figure 4-16), and adjust setscrew for slight drag of disk pack.

FEELER GAUGE   SETSCREW

Figure 4-16. Sector/Index Transducer Adjustment
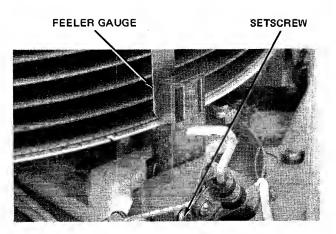
s. Perform radial alignment check. Refer to Section 5 of this manual.

POSITIONING SYSTEM

a. Remove air shroud.

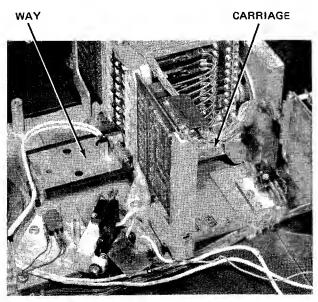b. Inspect carriage and way (see Figure 4-17).

WAY   CARRIAGE

Figure 4-17. Carriage and Way

c. Remove grease and dirt from carriage and way surfaces.

d. Lubricate carriage way, along roller bearing surfaces.

e. Inspect index rack for dirt and dust, and clean rack with alcohol-dampened swab.

f. Apply rust-preventing silicon-lube to lint-free cloth and apply to index rack.

g. Install air shroud.

h. Install a scratch disk pack.

i. Install disk drive exerciser and power-up disk drive.

j. Check power supply output voltages listed in Table 4-1.

Table 4-1. Power Supply Output Voltages

Voltage	Pin
+45 vdc	15B56
+36 vdc	15B53
+24 vdc	15B58
+ 5 vdc	15B60
- 24 vdc	15B55

k. Connect oscilloscope in accordance with information given in Figure 4-18. Check oscillator output.

PROG: 100 kHz OSCillator Check
SYNC: Ext   Pos   10 us   TRIG
CHAN: 1   DC   1 v   06B01   100 kHz OSC
CHAN:
MODE: **CHAN 1** only
NOTE: Signal must be +2.5 v above and -2.5 v below ground (5 v pk-pk).
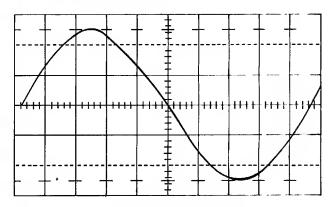

Figure 4-18. Oscillator Check

l. Adjust oscillator potentiometer (06B), if necessary, to obtain correct amplitude.

m. Check dc offset (see Figure 4-19).

PROG: Repetitive Single Cylinder Seeks
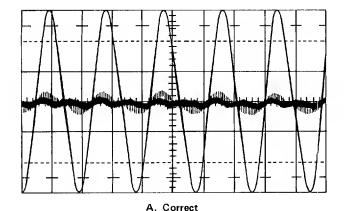SYNC: Ext   Pos   5 μs   06B01   100 kHz OSC
CHAN: 1   DC   100 mv   05C04   CYLXDUCER
CHAN:
MODE: **CHAN 1** only
NOTE: Signal centerline should not have any overlap.

A. Correct

B. Incorrect

Figure 4-20. Null Check

B. Incorrect

Figure 4-19. Dc Offset Check

p. Adjust demodulator NULL potentiometer (05C-closets to pins), if necessary, to obtain minimum null.
Check position gain (see Figure 4-21).
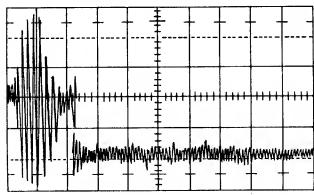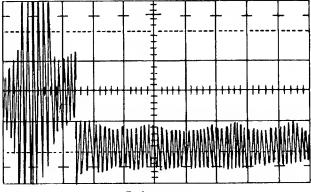
PROG:	Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 ms	09A05	SKFWD
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:	2	DC	2 v	02B26	GTDATN
MODE:	Added				
NOTE:	Null at gated attention time must be less than 130 millivolts.				

n. Adjust servo preamplifier OFFSET potentiometer (13A-top), if necessary, to obtain correct balance.

o. Check null (see Figure 4-20).

PROG:	Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 μs	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	Signal centerline should be reasonably flat.				

A. Correct

A. Correct

B. Incorrect

Figure 4-21. Position Gain Check

r. Adjust demodulator POSITION GAIN potentiometer (05C-furthest from pins), if necessary to obtain correct gain.

s. Check maximum velocity (see Figure 4-22).

PROG: Repetitive 203 Cylinder Seeks
SYNC: Ext Pos&Neg 10 ms 09A05 SKFWD
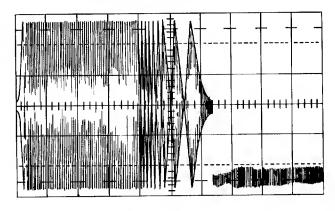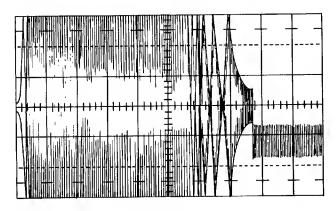CHAN: 1 DC 100 mv 05C04 CYLXDUCER
CHAN: 2 DC 2 v 02B26 GTDATN
MODE: Added
NOTE: Time to gated attention must not be greater than 65 milliseconds, or less than 60.

A. Correct

B. Incorrect

Figure 4-22. Velocity Check

READ/WRITE SYSTEM

a. Program exerciser to perform a write of "1's" on cylinder 000, all heads (00-19).

b. Program exerciser to perform a read on cylinder 000, all heads (00—19).

c. Monitor read data and observe a minimum amplitude of 150 millivolts.

SYNC: Int Pos 1 ms AUTO
CHAN: 1 AC 50 mv 02C13 RDDATA
CHAN: 2 AC 50 mv 02C15 RDDATA/
MODE: CHAN 2 inverted and added

d. If a read/write head has an output amplitude of less than 150 millivolts it must be replaced.

e. Program the exerciser to perform a write of "1's" on cylinder 202, all heads (00—19).

f. Program exerciser to perform a read at cylinder 202, all heads (00—19).

g. Monitor read data and observe minimum amplitude of 75 millivolts (for "1's" data only).

SYNC: Int Pos 1 ms AUTO
CHAN: 1 AC 50 mv 02C13 RDDATA
CHAN: 2 AC 50 mv 02C15 RDDATA/
MODE: CHAN 2 inverted and added

h. If a read/write head has an output amplitude of less than 75 millivolts it must be replaced.

i. Power-down disk drive, remove ac power, and remove disk pack.

j. With a VOM, check for continuity from support bracket of read/write head to deck plate. Reading observed should be less than 0.5 ohm. If reading is more than 0.5 ohm, investigate cause.

t. Adjust servo preamplifier VELOCITY potentiometer (13A-bottom), if necessary, to obtain correct velocity.

SECTION 5

CHECKS, ADJUSTMENTS AND REPLACEMENTS

GENERAL

The information contained in this section describes the procedures for performing operational checks, alignments and adjustments, and removal and replacements on the disk drive.

NOTE

It is recommended that maintenance personnel read the entire check, adjustment, or replacement procedure prior to performing the procedure to fully understand the scope of the task at hand.

DISK DRIVE SYSTEM

The disk drive system is made up of a cabinet and a single disk drive. The cabinet contains the power supply, power distribution panel, interface connector panel and operator controls. The drive contains a spindle system, positioning system, read/write system, and air filtration system (see Figure 5-1).

CABINET SYSTEM

The cabinet system houses the disk drive and contains the following components (see Figures 5-1 through 5-3).

- Operator's Control Panel

- Interface Connector Panel

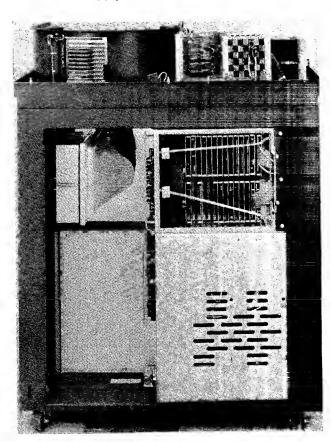- Power Distribution Panel

- Power Supply

Figure 5-1. Disk Drive, Front and Rear Views (Covers Removed)

OPERATOR CONTROL PANEL (Standard Model)

The operator control panel contains controls and indicators for the system (see Figure 5-2).
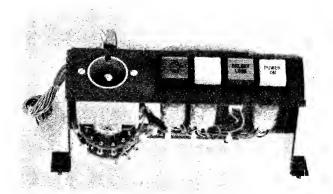

Figure 5-2. Operator Control Panel (Standard)

The components on the operator control panel are:

- Control and indicator panel
- Identification plug and switches
- Identification plug microswitch

Control and Indicator Panel

The controls and indicators for the standard disk drive are described in Table 5-1.

Table 5-1. Controls and Indicators, Standard Model

Control/Indicator	Description/Function
POWER ON Switch	Pushbutton switch used to initiate a power-Pushbutton switch used to initiate a power-up or power-down sequence.
SELECT LOCK Indicator (Red)	Indicates that an unsafe condition exists and that corrective action is required.
FILE LETTER Indicator (Green)	Indicates that the initial seek is completed and that the drive is ready for operation.

Identification Plug and Switches

The identification plug is a removable plug on which is inserted an identification number. The digit identifies the logical address of the unit (0 to 7, or S-spare). When the tog cover is removed the identification plug switches can be observed (see Figure 5-3).

When the plug is installed the disk drive is identified to a controller by the digit (0 to 7, or S-spare). Each identification plug is keyed differently by a stand-off on the side of the plug, which slides into the switch, when the switch is rotated to the correct position. Unit numbers can be reassigned by exchanging plugs. A unit with its plug removed is off-line.

IDENTIFICATION
PLUG SWITCHES
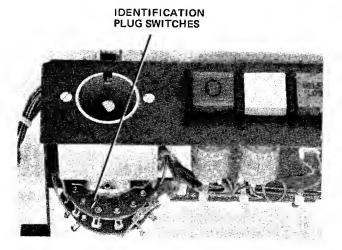
Figure 5-3. Identification Plug Switches

Identification Plug Microswitch

The identification plug microswitch monitors the presence or absence of the identification plug. The absence of the plug indicates that the disk drive is in an off-line condition. The presence of the plug enables on-line operations of the disk drive.

OPERATOR CONTROL PANEL (OEM Model)

The operator control panel (Figure 5-4) contains controls and indicators for the system.

Figure 5-4. Operator Control Panel (OEM)

The controls and indicators for OEM disk drives are described in Table 5-2.

Materials required to perform the following procedures are:

- Wrenches (3/16- and 1/4-inch)

Table 5-2. Controls and Indicators, OEM Models

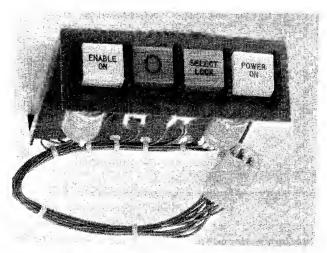| Control/Indicator	Description/Function
POWER ON Switch	Pushbutton switch used to initiate a power-up or power-down sequence.
READY Indicator (Green)	Indicates that the initial seek is completed and that the drive is ready for operation.
SELECT LOCK Indicator (Red)	Indicates that an unsafe condition exists and that corrective action is required.
READ ONLY Indicator (Yellow)	Indicates the state of the READ ONLY switch as to whether the driver's write logic is inhibited (lighted); or not inhibited (unlighted).
READ ONLY Switch	Pushbutton switch used to disable the driver's write logic; the state of which is monitored by the READ ONLY indicator.

Operator Control Panel Check

a. Check for proper operation of switches on control and indicator panel.

b. Remove control panel cover.

c. Observe identification (ID) plug microswitch as ID plug is removed and installed.

d. Disk drive should perform restore operation when ID plug is removed and installed.

Operator Control Panel Adjustments

a. Power-down disk drive and remove control panel cover.

b. Adjust ID plug microswitch to ensure contact closure when ID plug is fully inserted (see Figure 5-5).

ID PLUG
MICROSWITCH
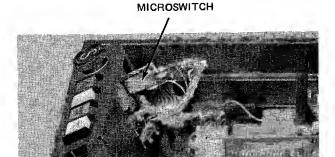
Figure 5-5. Identification Plug Microswitch

Operator Control Panel Replacement

a. Remove ac power and remove control panel cover.

b. Loosen four screws fastening panel to cabinet (see Figure 5-6).
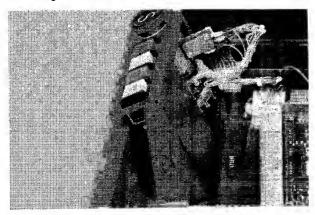
Figure 5-6. Operator Control Panel

c. Remove connecting plug.

d. Remove hold-down nuts and remove module.

e. To install replacement module, reverse procedure.

INTERFACE CONNECTOR PANEL

The interface connector panel is located in the front bottom of the cabinet (see Figure 5-7).
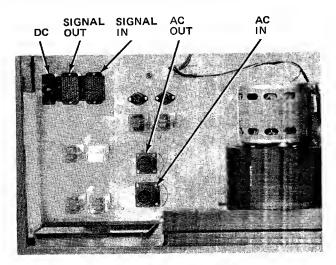
Figure 5-7. Interface Connector Panel

The upper left-hand side of the connector panel contains the I/O Connector Panel, which is the cable connector and the SIGNAL IN and SIGNAL OUT cable connectors. The lower center contains the AC IN and AC OUT cable connectors

POWER DISTRIBUTION PANEL

The power distribution panel distributes the 208/230 vac to the:

- Dc power supply
- Blower motor
- Spindle motor

Primary power switch S1 enables ac power to be distributed through the system (see Figure 5-8).

Figure 5-8. Power Distribution Panel

Material required to perform the following procedure is:

- Screwdriver

Power Distribution Panel Replacement

a. Remove ac power connector J1

b. Remove connectors P6 and P7.
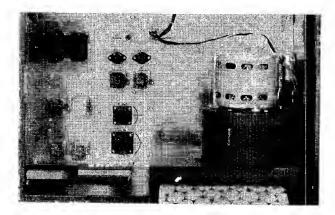
c. Remove six screws on outside of panel and carefully ease panel down.

d. If it is required to remove entire assembly, leads on terminal board must be labeled and removed.

e. If replacing panel, reverse procedure.

POWER SUPPLY

The power supply provides the following voltages for the disk drive.

- +45 vdc
- +24 vdc
- −24 vdc
- −24 vdc (servo)
- +5 vdc
- 24 vac

The power supply utilizes 208/230 vac ±10% single phase as input power. Two terminals are available on the terminal board for application of input power (see Figure 5-9).
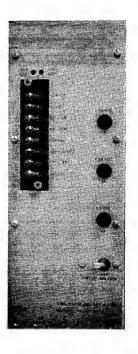
Figure 5-9. Power Supply

- Use 208 vac terminal if input power is 180 vac to 218,vac
- Use 230 vac terminal if input power is within 219 to 250 vac

NOTE

On earlier model units, the physical location of ac terminals differs from that shown in Figure 5-9.

Materials required to perform the following procedures are:

- Voltohmmeter
- Screwdriver

Power Supply Checks (Refer to Table 5-3 and 5-4)

Table 5-3. Resistance Checks

Terminal	Load	No Load
+45 VDC	200 ohms	00 ohms
+24 VDC	24 ohms	740 ohms
-24 VDC	6 ohms	600 ohms
-24 SERVO	6 ohms	600 ohms
+ 5 V	22 ohms	2,200 ohms

Table 5-4. Voltage Checks

Terminal	Remarks
208/230 VAC ±10%	Single phase input power
+45 V +5%, -10%	
+24 V ±5%	
- 24 V ±2%	(Adjustable)
- 24 V SVO ±5%	
+ 5 V ±1%	(Adjustable)
32 VAC rms (24)	Output is chopped sinewave

Power Supply Adjustment

a. Adjust the +5 V ADJ potentiometer for +5.0 ±1% vdc.

Power Supply Replacement

a. Set AC POWER switch S1 to OFF.

b. Remove plastic covers over terminal boards TB1 and TB2.

c. Disconnect and label wires from terminal boards, one at a time, for subsequent reconnection.

d. Remove eight screws fastening power supply to swing frame.

e. Remove power supply.

CAUTION

The power supply is heavy and cumbersome. Use care in handling.

f. To install replacement power supply, reverse procedure.

g. Perform resistance checks prior to applying power.

h. Apply power and perform voltage checks and adjustments.

SPINDLE SYSTEM

The spindle system comprises the following:

● Pack switch

● Spindle grounding brush

● Spindle assembly

● Spindle belt

● Spindle drive motor and pulley

● Sector/Index transducer

● Spindle lock and linkage shaft

Two components of the spindle system may be observed above the deck plate assembly (see Figure 5-10).

● Spindle

● Sector/Index Transducer
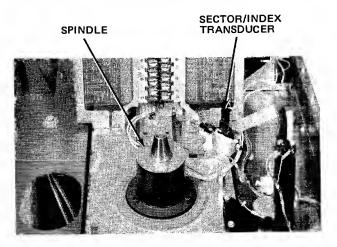
Figure 5-10. Spindle System Components

The remainder of the spindle can be observed from below the deck plate assembly (see Figure 5-11).

● Pack-On Switch

● Spindle Grounding Brush

● Spindle Drive Belt

● Spindle Motor Pulley (not shown)

● Spindle Lock and Linkage Shaft

● Spindle Drive Motor
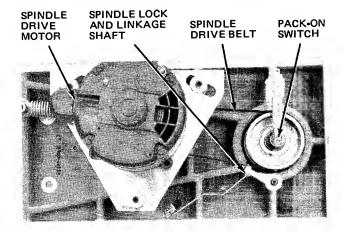
Figure 5-11. Spindle System Components, Lower

The spindle drive motor is mounted on the underside of the deck plate and is connected to the spindle assembly by a friction drive belt. The spindle assembly is mounted on top of the deck plate, with the sector/index transducer.

The task of the spindle system is to rotate the disk pack at a rate of 2400 ±48 revolutions per minute. When the disk pack is installed on the spindle, the spindle locking mechanism closes the interlock contacts of the pack switch. With all interlocks closed, and power applied, the spindle motor starts to rotate the spindle assembly and the disk pack.

The sector/index transducer detects each index notch machined into the periphery of the sector/index disk, as the disk pack rotates. The transducer is mounted on a hinged assembly so that when the disk pack is installed, and the access door is closed, the transducer tilt bracket positions the transducer over the periphery of the sector/index disk for index notch detection.

PACK SWITCH

The pack switch is an integral part of the disk drive's power-up sequence. The task is twofold to:

- Indicate the presence of a disk pack mounted on the spindle

- Provide a ground path for the static discharge from the spindle to the deck plate

When the disk pack is installed on the spindle, the spindle shaft rises closing the pack switch contacts. When the disk pack is removed from the spindle, the spindle shaft drops forcing the switch contacts to open.

Materials required to perform the following procedures are:

- Long-nosed pliers
- Gram gauge (0-500 grams)
- Hex-head wrench (5/32-inch)
- Common screwdriver

Pack Switch Operational Checks

a. With disk pack removed, ensure that pack switch contacts are open.

b. With disk pack installed, ensure that pack switch contacts are closed.

c. With disk pack installed, tension required to open lower contact is 100 ±5 grams (see Figure 5-12).

d. To adjust, form contact arm.

e. Recheck opening and closing of pack switch.

f. Check tension on spindle grounding brush contact arm. With disk pack installed, approximately 300 to 500 grams are required to open brush contact (see Figure 5-12).
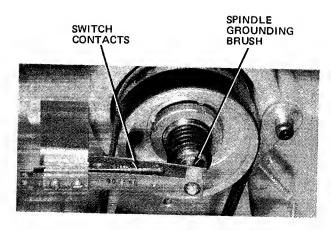

Figure 5-12. Pack Switch Assembly

Pack Switch Replacement

a. Remove push-on connection wires from pack switch.

b. Remove and replace pack switch assembly by removing hex-head bolts that fasten assembly to deck plate.

c. After replacement, recheck operation of assembly.

NOTE
It is recommended that the pack switch be replaced as an assembly.

SPINDLE GROUNDING BRUSH

The spindle grounding brush provides a static discharge path for the disk pack and spindle. The brush is fastened to the base of the spindle shaft and provides ground continuity for the spindle to the deck plate through the brush contact arm of the pack switch assembly.

Materials required to perform the spindle grounding brush procedures are:

- Voltohmmeter
- Emery cloth (fine)
- Hex-head wrench (0.050-inch)
- Hex-head wrench (5/32-inch)

Spindle Grounding Brush Operation Check

a. With power on and disk pack spinning, check for continuity from rotating grounding brush, to brush contact arm (see Figure 5-13).
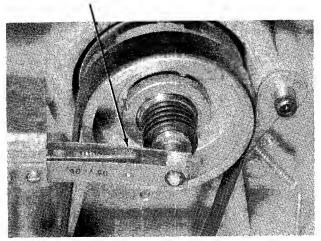
Figure 5-13. Spindle Grounding Brush Check

b. If resistance exceeds one ohm, clean the grounding brush and contact with fine emery cloth.

Spindle Grounding Brush Replacement

a. Loosen pack switch assembly from deck plate enough to allow contact arms to pivot past grounding brush.

b. Loosen set screw and remove grounding brush from spindle shaft.

c. Install new grounding brush using existing set screw.

SPINDLE ASSEMBLY

The spindle assembly is mounted in the deck plate and is used to hold and rotate the disk pack (see Figure 5-14).
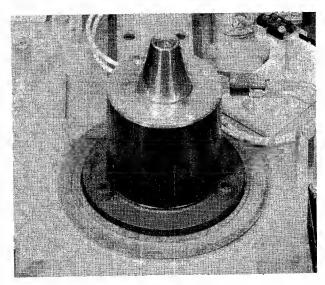

Figure 5-14. Spindle Assembly

Materials required to perform the following procedures are:

- Loctite
- Hex-head wrenches (0.050- and 1/4-inch)
- Cotton-tipped swab
- Alcohol (91%)
- Sta-Lube Molybdenum grease
- Brush
- Spring Scale (0 — 40 pounds)

Spindle Operational Checks

a. Ensure that disk pack slides onto drive spindle smoothly and tightens firmly.

b. Ensure that disk pack can be removed from drive spindle smoothly.

Spindle Replacement

a. Remove three bolts fastening spindle to deck plate. Clean old Loctite from bolts.

b. Remove spindle assembly from deck plate by pulling spindle assembly straight up.

CAUTION

The spindle and deck plate are machined to extremely close tolerances. Cocking the spindle will result in binding against the deck plate and may damage the machined surfaces.

c. Replace drive spindle as an assembly. Remove grounding brush and install on replacement spindle shaft.

d. Check read/write head alignment.

SPINDLE BELT

Spindle Belt Tension Check

a. Connect spring scale to measure spring tension.

b. Pull spring scale toward the right of the cabinet.

c. Ensure that tension required to pull motor toward spindle is not less than 14 pounds.

d. Ensure that drive belt is running in center of pulleys.

Spindle Belt Replacement

a. Pull drive motor toward spindle assembly until belt is loose enough to slip off motor pulley.

b. Allow drive belt to drop from spindle drive system pulleys.

c. To install new belt, reverse procedure.

d. Spin drive belt and ensure that belt rides in center of both pulleys.

SPINDLE DRIVE MOTOR AND PULLEY

The spindle drive motor is a capacitor start motor. The motor provides high starting torque at low speed. As the motor accelerates an internal centrifugal switch disconnects the start winding for a normal full speed of 3670 rpm for 60 Hz, or 2970 rpm for 50 Hz (3450 and 2850 is at rated load for 60 Hz and 50 Hz, respectively).

By utilizing different diameter pulleys for the drive motor, the rotational speed of the spindle is 2400 rpm (±48 rpm).

Materials required to perform the following procedure are:

● Hex-head wrench (5/16- and 9/16-inch)

● Screwdriver

Spindle Drive Motor Replacement

a. Disconnect spindle drive motor power.

b. Remove cover at side of motor and disconnect wires from motor.

c. Pull drive motor toward spindle and slip drive belt off motor pulley.

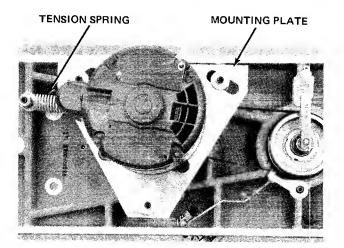d. Remove four bolts fastening drive motor to drive motor mounting plate (see Figure 5-15).

Figure 5-15. Spindle Motor Mounting Plate

e. Remove drive motor.

f. Remove motor pulley from end of drive shaft.

g. Install motor pulley on drive shaft of new motor. Approximately 3/16-inch shaft should protrude past pulley face. Replace and tighten pulley retaining screw.

h. Install replacement motor in mounting plate.

i. Install spindle drive belt.

j. Connect wiring to new drive motor and replace cover.

k. Spin drive spindle pulley to ensure drive belt runs straight and true. Belt adjustment is not necessary.

l. Install scratch disk pack, set AC POWER switch to ON, power-up disk drive, and ensure disk pack rotation is counterclockwise.

SECTOR/INDEX TRANSDUCER

The sector/index transducer (Figure 5-16) detects slots in timing disk of the disk pack and generates a pulse for each slot when the disk pack is rotating.
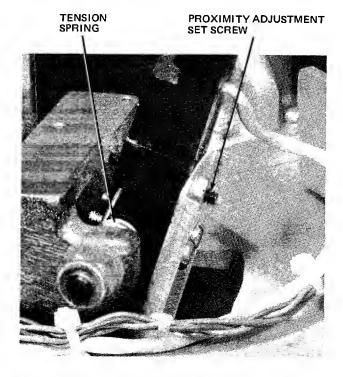

Figure 5-16. Sector/Index Transducer Adjustment

Materials required to perform the following procedures are:

● Transducer alignment tool

● Screwdriver

● Hex-head wrench

● Oscilloscope

● Crescent wrench (4-inch)

Sector/Index Transducer Check

a. Remove air shroud.

b. Install alignment tool on spindle.

c. Adjustable set screw must touch the transducer mount while check is being made.

Sector/Index Transducer Operational Check

a. Install scratch pack.

b. Power-up disk drive.

c. Monitor index pulses (see Figure 5-17).

```
PROG:   Index Pulse Repetition Rate Check
SYNC:   Int    Neg    5 ms      TRIG
CHAN:   1      DC     1 v       06C13    INDEX
CHAN:
MODE:   CHAN 1 only
NOTE:   Repetition rate must be 25 milliseconds.
```
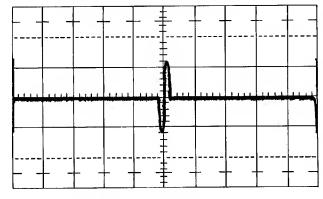

Figure 5-17. Index Pulse Repetition Rate

d. Index pulses should be 25 milliseconds apart.

e. Increase sweep time to 5 microseconds (see Figure 5-18).

```
PROG:   Index Pulse Polarity Check
SYNC:   Int    Neg    5 µs      TRIG
CHAN:   1      DC     1 v       06C13    INDEX
CHAN:
MODE:   CHAN 1 only
NOTE:   Index must go negative prior to making negative to
        positive transition.
```
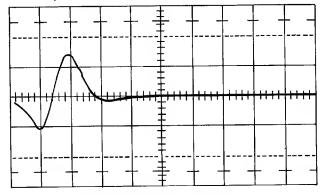

Figure 5-18. Index Pulse Polarity

f. Observe that leading edge of index pulse waveform goes negative before going positive. If waveform is inverted power-down, reverse transducer leads, and power-up to continue check.

g. Observe pulses for amplitude; minimum peak-to-peak amplitude is 1.3 volts; maximum peak-to-peak amplitude is 2.25 volts.

Sector/Index Transducer Replacement

a. Remove air shroud.

b. Remove two screws and locknut holding tilt bracket to transducer (see Figure 5-19).

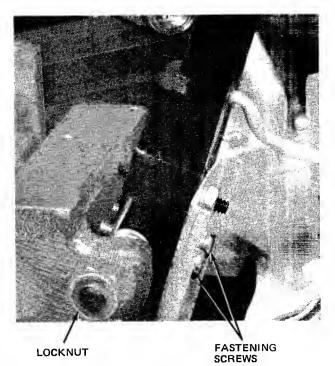LOCKNUT   FASTENING
                           SCREWS

Figure 5-19. Sector/Index Transducer Replacement

c. Remove one end of tension spring from slot in transducer and remove transducer.

d. Place replacement transducer against shaft.

e. Position tilt bracket on transducer and install locknut on adjusting screw.

f. Insert and tighten the two screws that fasten the tilt bracket to transducer.

g. Place tension spring arm into slot on transducer.

h. Ensure that tension spring is not tightly compressed between mounting block and transducer. If so, loosen two screws fastening mounting block to deck plate and move block away from read/write heads.

i. Tighten both mounting screws.

j. Perform transducer mechanical and operational checks.

k. Perform radial adjustment procedure.

SPINDLE LOCK AND LINKAGE SHAFT

The spindle lock prevents the drive spindle from rotating while the pack access door is in the open position. The mechanical linkage engages when opening the pack access cover. The linkage pushes a locking arm into a detent notch in the spindle pulley thereby locking the spindle shaft, also moving the index transducer away from the pack.

Materials required to perform the following procedures are:

• Hex-head wrench (5/32-inch)

• Crescent wrench (4-inch)

• Screwdrivers

Spindle Lock Operational Check

a. Open disk pack access door and attempt to rotate spindle.

b. Spindle should be locked or should lock after small rotational movement of spindle.

c. Close access door and check spindle for free rotation by rotating spindle.

d. If locking mechanism does not operate properly, adjust spindle lock by forming mechanical linkage as required (see Figure 5-20).
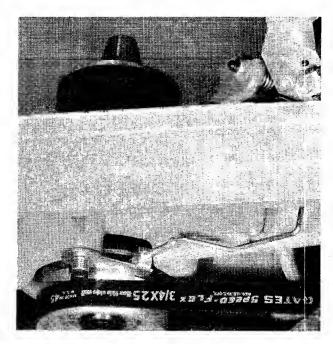

Figure 5-20. Spindle Linkage Shaft

e. Observe that spindle lock has complete freedom of movement.

f. Install disk pack and ensure that spindle lock engages.

g. Close disk pack access door.

h. Ensure that spindle spins freely.

i. Remove disk pack.

Spindle Lock and Linkage Shaft Replacement

a. Remove air shroud.

b. Remove hex-head screw that fastens spindle locking bracket to underside of deck plate.

c. Remove ring retaining clip holding locking bracket to linkage shaft (see Figure 5-21).

Figure 5-21. Spindle Lock Retaining Clips

d. To install linkage shaft, reverse procedure.

e. Perform rack end microswitch adjustment.

f. Install air shroud and perform sector/index transducer adjustments.

g. Perform radial adjustment procedure.

POSITIONING SYSTEM

The positioning system is an electromagnetic-mechanical device that has the task of moving the read/write heads (see Figure 5-22).
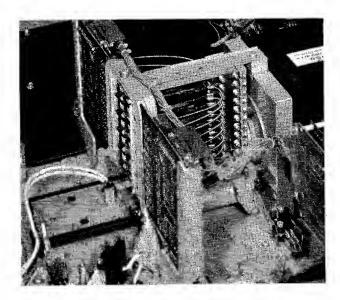
Figure 5-22. Positioning System

The positioning system can be subdivided into three basic functions:

- Electronic
- Magnetic
- Mechanical

The magnetic and mechanical portion of the system is defined as follows:

- Magnetic — Linear Motor Assembly
- Mechanical — Carriage and Way Assembly

The linear motor assembly provides the drive for the positioning system and comprises the following:

- Motor Magnet
- Bobbin and Conductor Bands
- Velocity Transducer:
  - Velocity Tachometer Rod
  - Velocity Tachometer Rod Housing

The carriage and way assembly provides a stable mounting platform for the read/write heads and comprises the following:

- Carriage Way
- Carriage and Head Mounting Block
- Index Rack
- Cylinder Transducer

Materials required to perform the following positioning system checks are:

- Oscilloscope
- Disk Drive Exerciser

POSITIONING SYSTEM CHECKS

a. Remove ac power by setting AC POWER switch S1 to OFF.

b. Install a disk drive exerciser and a disk pack.

c. Power-up disk drive.

d. Monitor output of 100 kiloHertz oscillator (see Figure 5-23).

PROG: 100 kHz OSC Check and Adjustment
SYNC: Int   Pos   10 µs   TRIG
CHAN: 1   DC   1 v   06B01   CYLXDUCER
CHAN:
MODE: CHAN 1 only
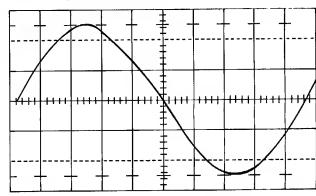NOTE: Signal must be +2.5 v above and -2.5 v below ground (5 v p/p).

Figure 5-23. 100 kHz OSC Check

e. Program exerciser to perform repetitive single cylinder seeks forward and reverse.

f. Monitor output of cylinder transducer (see Figure 5-24).

PROG: Repetitive Single Cylinder Seeks
SYNC: Ext   Pos   5 ms   09A05   SKFWD
CHAN: 1   DC   100 mv   13A31   CYLXDUCER
CHAN:
MODE: CHAN 1 only
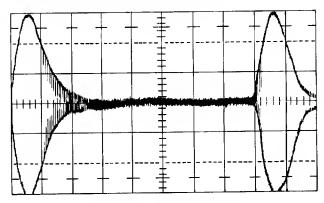NOTE: 40 millisecond nulls between seeks.

Figure 5-24. 40-Millisecond Nulls

g. Adjust repetition rate on exerciser for approximately 40 milliseconds between seeks.

h. Check servo offset (see Figure 5-25).

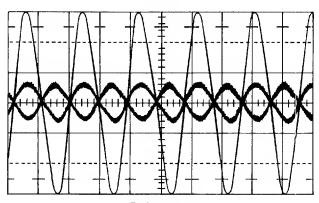| PROG:	Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 μs	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	13A31	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	Overlapping signals must be in phase. If adjustment is required see Servo Adjustments, this section.				
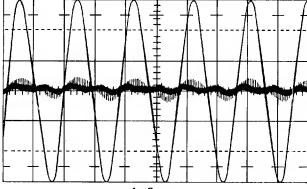
A. Correct

B. Incorrect

Figure 5-25. Offset Check

i. Check servo null (see Figure 5-26).

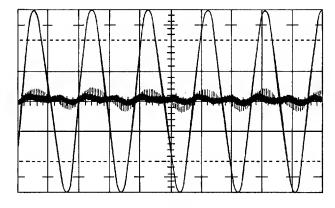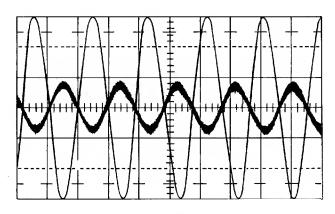| PROG:	Repetitive Single Cylinder Seeks - 40 millisecond nulls between seeks				
SYNC:	Ext	Pos	5 μs	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	Signal must be reasonably flat. If adjustment is required see Servo Adjustments, this section.				

A. Correct

B. Incorrect

Figure 5-26. Null Check

j. Check cylinder transducer gain (see Figure 5-27).

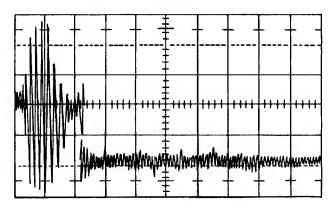| PROG:	Repetitive Single Cylinder Seeks - 40 millisecond nulls between seeks				
SYNC:	Ext	Pos	5 ms	09A05	SKFWD
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:	2	DC	2 v	02B26	GTDATN
MODE:	Added				
NOTE:	Gain must be less than 130 millivolts at GTDATN time. If adjustment is required, see Servo Adjustments, this section.				

A. Correct

B. Incorrect

Figure 5-27. Cylinder Transducer Gain Check
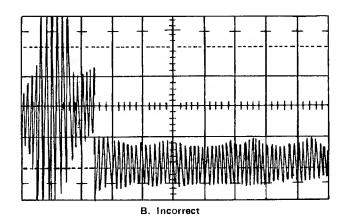

C. Amplitude Too Low

Figure 5-28. Cylinder Transducer Amplitude Check

k. Check cylinder transducer amplitude (see Figure 5-28).

PROG: Repetitive 203 Cylinder Seeks
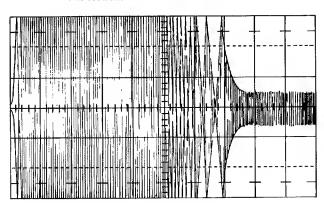SYNC: Ext   Pos   10 ms   09A05   SKFWD
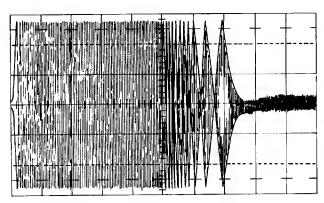CHAN: 1   DC   200 mv 05C04   CYLXDUCER
CHAN:
MODE: CHAN 1 only
NOTE: Amplitude must be greater than 600 millivolts and less than 1000 millivolts. If adjustment is required, see Cylinder Transducer Adjustment, this section.
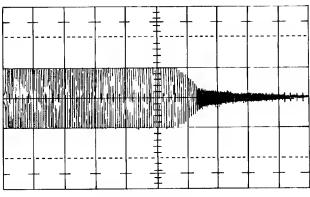
l. Check cylinder transducer/index rack alignment (see Figure 5-29).

PROG: Repetitive 203 Cylinder Seeks
SYNC: Ext   Pos   10 ms   09A05   SKFWD
CHAN: 1   DC   100 mv 05C04   CYLXDUCER
CHAN:
MODE: CHAN 1 only, multiplied X10
NOTE: Tooth-to-tooth relationship of adjacent teeth must be within 20% of each other (p/p). If adjustment is required, see Cylinder Transducer/ Index Rack Adjustments, this section.

A. Amplitude Too High

A. Correct

B. Correct

B. Incorrect

Figure 5-29. Cylinder Transducer/Index Rack Alignment Check

m. Check end-to-end variation of cylinder transducer/index rack alignment (see Figure 5-30).

PROG: Repetitive 203 Cylinder Seeks

SYNC: Ext   Pos   10 ms   09A05   SKFWD

CHAN: 1   DC   100 mv   05C04   CYLXDUCER

CHAN:

MODE: CHAN 1 only

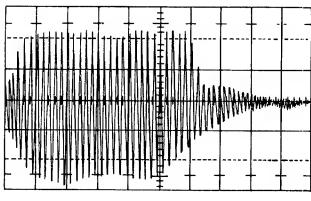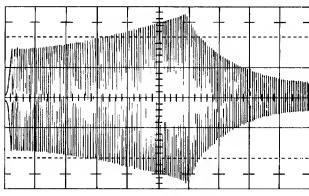NOTE: End-to-end variation must not exceed 300 milli-volts. If adjustment is required, see Index Rack Adjustment, this section.

A. Correct

B. Incorrect

Figure 5-30. End-to-End Variation

n. Check velocity of positioning system (see Figure 5-31).

PROG: Repetitive 203 Cylinder Seeks
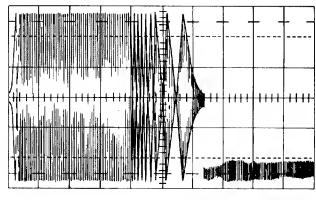
SYNC: Ext   Pos   10 ms   09A05   SKFWD

CHAN: 1   DC   100 mv   05C04   CYLXDUCER

CHAN: 2   DC   5 v   02B26   GTDATN

MODE: Added
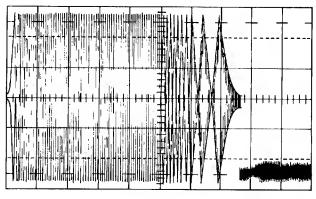
NOTE: Velocity is 65 milliseconds (-5 +0) to gated attention. If adjustment is required, see Servo Adjustments, this section.

A. Correct

B. Incorrect

Figure 5-31. Velocity Check

o. Change trigger slope from POS to NEG and check velocity again.

p. Remove ac power, remove disk drive exerciser.

q. Return disk drive to normal mode of operation.

CYLINDER TRANSDUCER

The cylinder transducer monitors the relationship between the transducer and the index rack to provide signals from which cylinder positions are determined.

Materials required to perform the following procedures are:

- Oscilloscope
- Disk Drive Exerciser
- Cylinder Transducer alignment tool
- Loctite
- Hex-head wrenches (1/16- and 7/64-inch)
- Head weights
- Alligator clip
- Grounding Wires
- Feeler gauge (0.015-inch)

Cylinder Transducer Preadjustment Procedure

a. Remove ac power by setting AC POWER switch S1 to OFF.

b. Replace read/write heads with head weights.

c. Remove spindle and blower motor plugs.

d. Jumper pack-on switch with alligator clip.

e. Jumper the following pins on selection unit:

09B19 to 09B03 (SPEED/) — implies up to SPEED

11A01 to 11A03 (SKERR*C) — disables SEEK ERROR

f. Install disk drive exerciser.

g. Remove hex-head screw fastening transducer to carriage way. Clean off all old Loctite. Apply small amount of fresh Loctite and replace screw. Tighten screw snugly but loose enough for transducer to be moved by alignment tool.

h. Install alignment tool perpendicular to rack. Loosen both setscrews until aligner balls are slightly inside tool. Mount the tool on the carriage way. Place feeler gauge between transducer and alignment tool and tighten hold-down screw on alignment tool (see Figure 5-32).
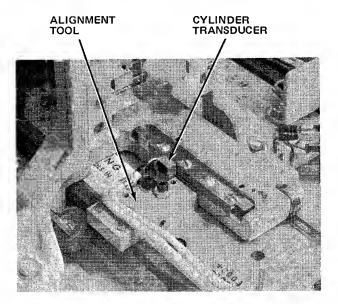

Figure 5-32. Cylinder Transducer Alignment Tool Installation

i. Remove servo amplifier module from location 15A and remove linear motor lead and tape it.

Cylinder Transducer Adjustment

a. Apply ac power. Do not power-up.

b. Check +5 volt output for +5 vdc ±1%.

c. Check 100 kHz oscillator (see Figure 5-33).

PROG: 100 kHz OSCillator Check

SYNC: Int   Pos   10 μs   TRIG

CHAN: 1   DC   1 v   06B01   100 kHz OSC

CHAN:

MODE: CHAN 1 only

NOTE: Signal must be +2.5 v above and -2.5 v below ground.
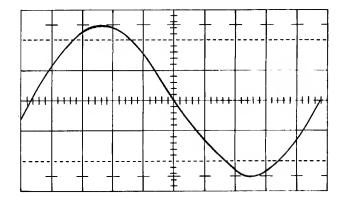
Figure 5-33. Oscillator Check

d. If oscillator output is incorrect, adjust potentiometer on oscillator module in location 06B.

e. Monitor output of cylinder transducer.

SYNC: Ext   Pos   10 ms   06B01   100 kHz OSC

CHAN: 1   DC   100 mv   05C04   CYLXDUCER

CHAN:

MODE: CHAN 1 only

f. Manually extend carriage and ensure that teeth on index rack do not touch cylinder transducer.

g. While moving index rack back and forth past transducer, adjust rear setscrew on alignment tool until transducer amplitude reaches approximately 400 millivolts (see Figure 5-34).
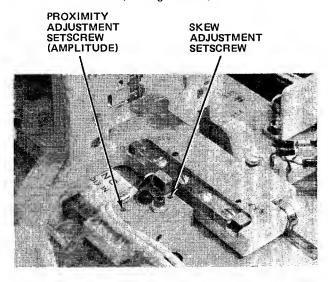
Figure 5-34. Cylinder Transducer, Rear Adjustment Screw

h. If variation from end-to-end exceeds 300 millivolts perform index rack adjustment.

i. Manually move index rack back and forth past transducer to check for equal cylinder-to-cylinder amplitude relationship across entire length of rack (see Figure 5-35).

PROG: Index Rack Linearity Check
SYNC: Ext Pos 10 ms 06B01 100 kHz OSC
CHAN: 1 DC 100 mv 05C04 CYLXDUCER
CHAN:
MODE: CHAN 1 only
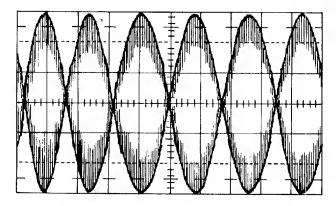NOTE: Amplitude must be within 300 millivolts from end-to-end.

Figure 5-35. Index Rack Amplitude

j. Adjust rear setscrew of cylinder transducer alignment tool and increase total amplitude to approximately 800 millivolts (600 − 1000 mv).

k. If transducer was replaced, phasing must also be checked.

l. Monitor output of servo preamplifier.

SYNC: Int Pos 1 ms AUTO
CHAN: 1 DC 5 v 13A35 SERVO
CHAN:
MODE: CHAN 1 only

m. Ground 07B49 (holds detent flip-flop set).

n. Position index rack so that cylinder transducer is on rack flat, approaching first tooth (see Figure 5-36).

o. Slowly move index rack so that transducer approaches first tooth.

p. Output of servo preamplifier must go negative. If not, reverse leads at 06C19 and 06C27.

q. Remove ground from 07B49.

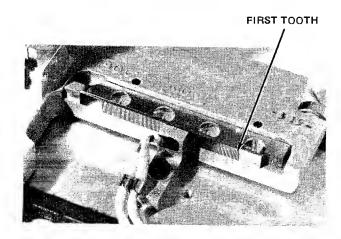r. Remove ac power and insert the servo amplifier in Location 15A.

FIRST TOOTH

Figure 5-36. Index Rack Flat and First Tooth

s. Remove lead from 09B03 and power-up disk drive.

t. After brush cycle begins, replace lead on 09B03.

u. At completion of brush cycle manually extend carriage to end stop.

v. Oscillate carriage back and forth. Position carriage so that cylinder transducer is at approximately center of rack.

w. Attach linear motor lead.

x. The carriage should detent.

y. Program exerciser to perform a RESTORE. Observe that carriage positions to cylinder 000.

z. Perform Servo Adjustments.

aa. Tighten retaining screw and recheck.

ab. Remove cylinder transducer alignment block.

ac. Remove jumper from pack-on switch 09B19 to 09B03, 11A01 to 11A03.

ad. Replace read/write heads.

ae. Perform read/write head alignment.

Cylinder Transducer Replacement

a. Remove ac power by setting AC POWER switch S1 to OFF.

b. Remove air shroud and read/write heads.

c. Remove cylinder transducer leads from pins:
*06C19
*06C27
*07C50
*07C52
*Remove ground leads

d. Cut cable clamps and remove cylinder transducer leads from deck plate.

e. Remove cable clamp.

f. Remove cylinder transducer holddown screw.

g. Remove cylinder transducer.

h. Clean Loctite from holddown screw and apply small amount of fresh Loctite.
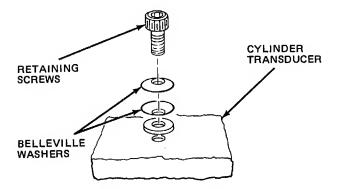
i. Install replacement transducer (see Figure 5-37).

Figure 5-37. Cylinder Transducer Installation

j. Replace cable clamp tie-down to transducer leads.

k. Connect cylinder transducer leads. One set of leads to 06C and the other set to 07C. Connect shield grounds to any convenient ground, pins 03 or 57 (see Table 5-5).

Table 5-5. Cylinder Transducer Lead Connections

Coil	Color	Pin
(PRI)	BLK	07C50
(PRI)	WHT	07C52
(PRI	YEL	06C57
(SEC)	RED	06C27
(SEC)	GRN	06C19
(SEC)	YEL	05C03

l. Perform cylinder transducer preadjustment procedure.

m. Perform cylinder transducer adjustment.

INDEX RACK

The relationship of the index rack to the cylinder transducer is monitored by the cylinder transducer. The signals developed are used to determine cylinder positions.

Materials required to perform the following procedures are:

- Oscilloscope
- Disk drive exerciser
- Loctite
- Hex-head wrench (1/16-inch).
- Screwdriver
- Alligator clip
- Grounding wires

Index Rack Preadjustment Procedures

a. Remove ac power by setting AC POWER switch S1 to OFF.

b. Replace read/write heads with head weights.

c. Remove spindle and blower motor plugs.

d. Jumper pack-on switch with alligator clip.

e. Jumper the following pins on selection unit:

09B19 to 09B03 (SPEED/) — implies up to SPEED
11A01 to 11A02 (SKERR*C) — disables SEEK ERROR

f. Install disk drive exerciser.

g. Remove servo amplifier module from Location 15A and remove linear motor lead and tape it.

Index Rack Adjustment

a. Remove four screws fastening index rack to carriage.

b. Clean off old Loctite residue and apply small amount of new Loctite. Install screws snugly.

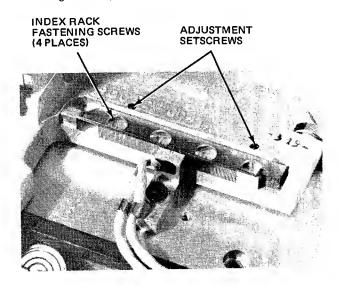c. Back off both adjustment setscrews to allow index rack to fit flush with the carriage (see Figure 5-38).

Figure 5-38. Index Rack Adjustment

d. Apply ac power.

e. Monitor cylinder transducer waveform.

SYNC:	Ext	Pos	10 ms	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				

f. Manually oscillate one end of index rack past cylinder transducer.

g. Adjust associated setscrew until observed amplitude is approximately 400 millivolts.

h. Manually oscillate other end of the index rack past cylinder transducer.

i. Adjust associated setscrew until observed amplitude is approximately 400 millivolts.

j. Manually oscillate entire index rack past cylinder transducer and ensure that amplitude is linear across entire rack; within 300 millivolts.

k. Perform cylinder transducer adjustment procedures.

Index Rack Replacement

a. Remove ac power.

b. Remove air shroud and read/write heads.

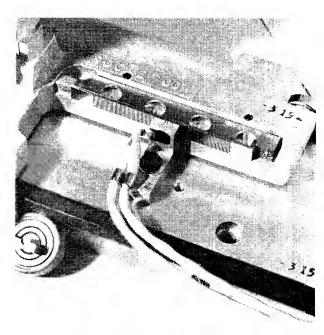c. Remove four screws fastening index rack to carriage. Remove index rack (see Figure 5-39).

Figure 5-39. Index Rack

d. Loosen adjusting setscrews and ensure adjustment balls are recessed inside carriage.

e. Install replacement index rack and apply Loctite to holddown bolts. Tighten screws snugly.

f. Perform index rack alignment procedures.

CARRIAGE AND WAY

The head mounting block is fastened to the carriage and provides a stable platform on which the read/write heads are mounted. The carriage is driven by the linear motor and utilizes the carriage way as a guide path to position the read/write heads in the rotating disk pack (see Figure 5-40).
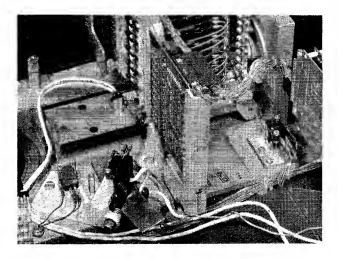
Figure 5-40. Read/Write Head Carriage

Materials required to perform the following procedures are:

• Dial Indicator

• Loctite

• Wrench, open end (3/16-inch)

• Hex-head wrench (1/4-inch)

• Spring Scale gauge (0 — 40 pounds)

• Head Weights

Carriage Pre-Tension Check

a. Remove ac power.

b. Remove air shroud.

c. If read/write heads are installed, insert two layers of lint-free paper between facing heads.

d. Mount dial indicator on air shroud standoff and manually extend carriage to end-stop (see Figure 5-41).

Figure 5-41. Dial Indicator Mounting

e. Place feeler end of dial indicator on center of ball bearing stud and preset dial indicator.

f. Utilizing spring scale, push edge of carriage toward dial indicator (see Figure 5-42).
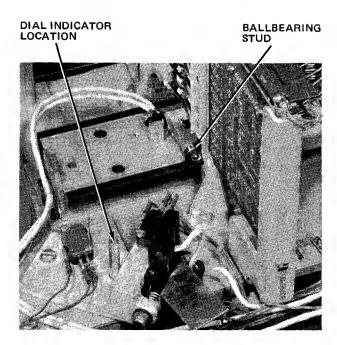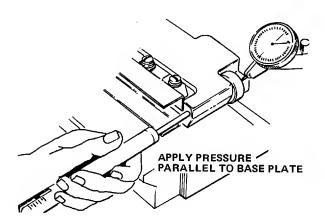

Figure 5-42. Carriage Pre-Tension Check

g. Observe that 9 to 10 pounds pressure are required to move carriage 0.001 to 0.002 inches.

Carriage Pre-Tension Adjustment

a. Remove roller guide bearing holddown bolt, clean off old Loctite.

b. Apply small amount of new Loctite and reinsert bolt.

c. Tighten roller guide bearing holddown bolt until pressure required to move carriage is 0.001 to 0.002 inches (9 to 10 pounds).

Carriage Replacement

a. Remove air shroud.

b. Remove read/write heads.

c. Remove head mounting block grounding strap.

d. Remove read preamplifiers and cam tower.

e. Remove three bolts holding bobbin to head block and carriage.

f. Remove velocity tach rod.

g. Disconnect cylinder transducer leads at 06C and 07C.

NOTE

The carriage and carriage way are matched assemblies and must be replaced as an assembly. A new, aligned, cylinder transducer is included.

h. Remove carriage and way assembly by removing four bolts fastening carriage way to deck plate.

i. Clean deck plate surfaces and remove old Loctite from four holddown screws.

j. Install replacement assembly on deck plate.

k. Replace velocity tach rod.

l. Replace bobbin.

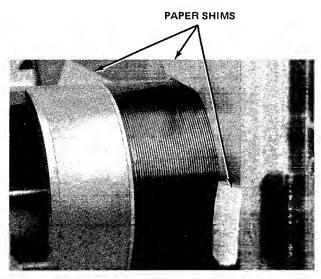m. Insert three pieces of shimstock, such as a computer card, at top and sides of motor bobbin (see Figure 5-43).

Figure 5-43. Bobbin Adjustment

n. Apply Loctite to three bolts and insert bolts. Longest bolt goes through head block.

o. Position bobbin as far into linear motor as possible and tighten bolts. Remove paper shims from bobbin and check that bobbin does not contact inside surface of linear motor.

p. Ensure that carriage rolls evenly and smoothly on carriage way.

q. Install head weights and perform cylinder transducer adjustments.

r. Replace cam tower and read preamps.

s. Replace the read/write heads and perform the read/write alignment procedures.

VELOCITY TRANSDUCER

The velocity transducer (Figure 5-44) comprises two assemblies:

• Velocity tachometer rod (magnet)
• Velocity tachometer rod housing (pickup coil)

Figure 5-44. Velocity Transducer

The velocity tach rod is fastened to the head mounting block and the tach rod housing is mounted inside the linear motor. As the carriage moves in either direction, the velocity tach rod moves inside the tach rod housing. The pickup coil then develops a control voltage which is applied to the positioning system as negative feedback.

Materials required to perform the following procedures are:

• Open-end wrench (3/16-inch)
• Loctite
• Oscilloscope
• Screwdriver (common)
• Diagonal pliers
• Plastic tie-downs

Velocity Tachometer Replacement

a. Remove ac power.

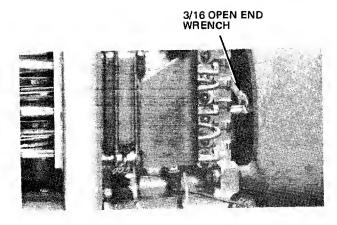b. Loosen tach rod from head mounting block, using a 3/16" open end wrench on the tach rod flats (see Figure 5-45).

3/16 OPEN END WRENCH

Figure 5-45. Velocity Tach Rod

c. Remove tach rod housing through rear of linear motor.

d. Ensure replacement tach rod is magnetized, then insert tach rod into tach rod housing.

e. Apply small amount of Loctite to threaded end of tach rod. Fasten rod to head block.

NOTE

Do not overtighten tach rod; it is possible to shear the tach rod.

f. Place two pieces of lint-free paper between facing read/write heads and manually extend head carriage.

g. Ensure that tach rod has complete freedom of movement within tach rod housing.

h. Check output of velocity transducer.

SYNC:	Int	Pos	1 ms	AUTO	
CHAN:	1	DC	1 v	13A05	VELTACH
CHAN:					
MODE:	CHAN 1 only				

i. Ensure that transducer output is positive in a forward direction and negative in a reverse direction.

j. If not, reverse transducer leads at pin locations 13A03 and 13A05.

k. Perform servo adjustments.

Velocity Tachometer Housing Replacement

a. Remove velocity tachometer rod.

b. Remove velocity tachometer housing plug.

c. Remove two screws holding housing retainer to rear of linear motor.

d. Remove housing, and housing tension spring inside motor.

e. Install replacement housing.

f. Install housing retainer.

g. Insert two pieces of lint-free paper between facing read/write heads.

h. Check output of velocity transducer.

SYNC: Int Pos 1 ms AUTO
CHAN: 1 DC 1 v 13A05 VELTACH
CHAN:
MODE: CHAN 1 only

i. Ensure that transducer output is positive in a forward direction and negative in a reverse direction.

j. If not, reverse transducer leads at pin locations 13A03 and 13A05.

k. Perform Servo Adjustments.

LINEAR MOTOR

The linear motor comprises a motor magnet block and a bobbin coil. The bobbin is fastened to the carriage and the complete assembly rides on the carriage way. When current is applied to the bobbin coil through flexible conductor bands, the coil reacts with the motor magnet's constant field and provides the driving force necessary to move the read/write heads forward or reverse.

Materials required to perform the following procedures are:

- Voltohmmeter
- Hex-head wrench (4/16-inch)
- Shim stock, 0.0025-inch (computer card or equivalent)
- Loctite
- Open-end wrench (3/16-inch)
- Screwdriver

Linear Motor Check

a. Remove ac power and remove linear motor lead (see Figure 5-46).
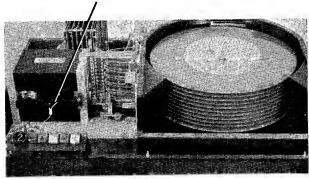
LINEAR MOTOR LEAD

Figure 5-46. Linear Motor Connector

b. Measure resistance of motor bobbin coil; it should be 3 ±0.5 ohms. Any measurement outside of these tolerances indicates a defective coil and the linear motor should be replaced.

c. Place two pieces of lint-free paper between each facing read/write head.

d. Measure for continuity to ground on both terminals of bobbin while moving carriage back and forth along entire carriage way. If continuity to ground exists, replace linear motor.

e. While moving carriage back and forth, ensure that conductor bands are not distorting and that bobbin is not rubbing against motor interior.

f. Position carriage at approximately cylinder position zero.

g. Connect an ammeter across bobbin terminals with positive lead connected to side nearest operator control panel.

h. Move carriage forward as rapidly as possible. Do not move carriage back until polarity of ammeter is reversed.

i. A good bobbin/motor magnet relationship will induce 600 to 675 milliamps. If reading is less than 525 milliamps, replace motor.

Bobbin Adjustment

a. Remove head 08.

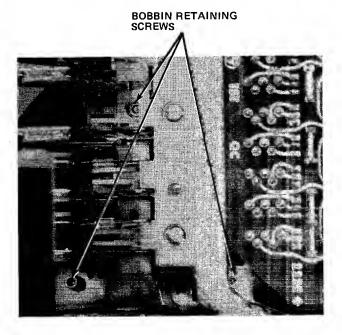b. Remove three screws fastening bobbin to carriage (see Figure 5-47).

BOBBIN RETAINING SCREWS

Figure 5-47. Bobbin Screws

c. Clean off old Loctite and apply small amount of new Loctite to threads of each screw. Reinstall screws loosely.

d. Place three pieces of shim stock (paper) around the outer flanges of bobbin, and carefully slide bobbin back into motor (see Figure 5-48).
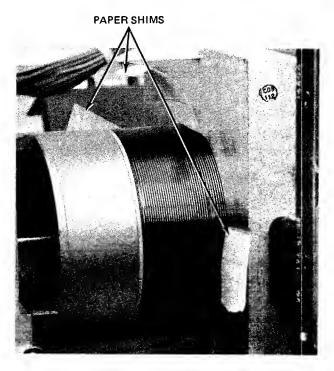
PAPER SHIMS

Figure 5-48. Bobbin Adjustment

e. Tighten all screws evenly.

f. Place lint-free paper between heads, extend carriage fully, and remove shim stock around bobbin.

g. Ensure that bobbin has complete freedom of movement within motor magnet and retract head carriage fully. Remove paper.

h. Reinstall head 08.

i. Perform final servo adjustment.

j. Perform read/write head alignment for head 08 only.

Motor Magnet Replacement

a. Remove ac power and linear motor leads.

b. Remove head 08.

c. Remove three bolts holding bobbin to head block.

d. Remove velocity tach rod and tach rod housing.

e. Remove three bolts holding linear motor to deck plate. Bolts are located underneath deck plate.

f. Remove motor from deck plate by grasping motor firmly and securely (see Figure 5-49).
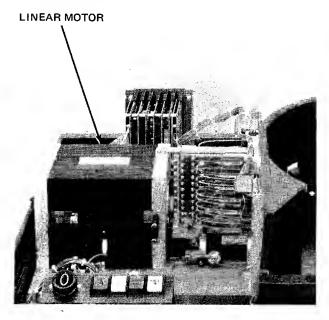
LINEAR MOTOR

Figure 5-49. Linear Motor

g. Motor bobbin may now be removed from motor magnet.

h. Install replacement motor by reversing procedure.

i. Clean deck plate surface and install new linear motor.

j. Install tach rod housing.

k. Install tach rod.

l. Perform bobbin adjustment.

m. Install head 08 and perform read/write head alignment procedure.

n. Install motor leads and perform Servo Adjustments.

Final Servo Adjustments

a. Monitor output of 100 kiloHertz oscillator (see Figure 5-50).

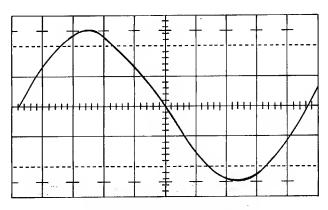|					
PROG:	100 kHz OSC Check and Adjustment				
SYNC:	Int	Pos	10 μs	TRIG	
CHAN:	1	DC	1 v	06B01	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	Signal must be +2.5 v above and -2.5 v below ground (5 v p/p).				

Figure 5-50. 100 kHz OSC Adjustment

b. Adjust potentiometer on the oscillator module, location 06B, for 5-volt peak-to-peak signal. Ensure that +5-volt output voltage is +5.0 volts ±1%.

c. Program disk drive exerciser to perform repetitive single cylinder seeks, alternate forward and reverse.

d. Monitor output of cylinder transducer (see Figure 5-51).

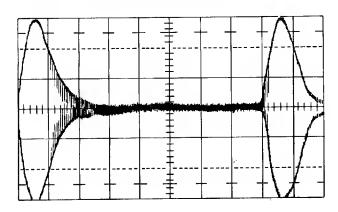| PROG:	· Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 ms	09A05	SKFWD
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	40 millisecond nulls between seeks.				

Figure 5-51. 40-Millisecond Null Adjustment

e. Adjust repetition rate potentiometer on exerciser for approximately 40 milliseconds between seeks.

f. Change sweep time and observe output of cylinder transducer during null time (see Figure 5-52). Offset adjustment may be required.

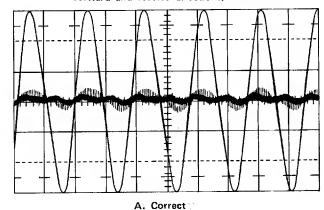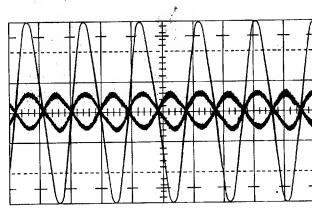| PROG:	Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 µs	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	The overlapping signals (centerline) must be in phase to ensure the offset is correct in both forward and reverse directions.				

A. Correct

B. Incorrect

Figure 5-52. Offset Adjustment

g. Adjust OFFSET potentiometer on servo preamplifier, location 13A, upper potentiometer.

h. Maintaining same scope settings observe and adjust null in the positioning system (see Figure 5-53).

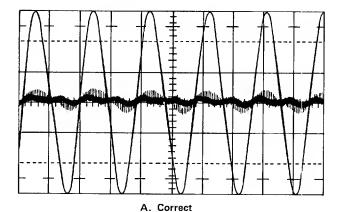| PROG:	Repetitive Single Cylinder Seeks				
SYNC:	Ext	Pos	5 µs	06B01	100 kHz OSC
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:					
MODE:	CHAN 1 only				
NOTE:	The balance (centerline) must be as flat as possible during the null time between seeks.				

A. Correct

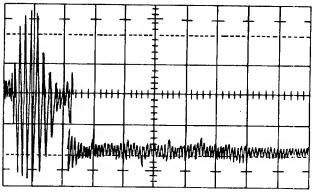B. Incorrect

Figure 5-54. Preliminary Gain Adjustment

B. Incorrect

Figure 5-53. Null Adjustment

i. Adjust the NULL potentiometer on the demodulator, location 05C, closest pot to pins.

j. Change scope settings and observe output of cylinder transducer gated attention time (see Figure 5-54).

PROG: Repetitive Single Cylinder Seeks
SYNC: Ext   Pos   5 ms   09A05   SKFWD
CHAN: 1   DC   100 mv 05C04   CYLXDUCER
CHAN: 2   DC   2 v   02B26   GTDATN
MODE: Added
NOTE: The output of the cylinder transducer at gated attention time must be less than 130 millivolts.
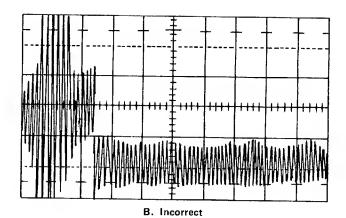

A. Correct

k. Adjust POSITION GAIN potentiometer on demodulator, location 05C, furthest pot from pins.

l. Change triggering slope from POS to NEG and repeat steps j and k. This ensures that gain is less than 130 millivolts in both forward and reverse directions.

NOTE

The subsequent steps are final gain adjustments and should be the best comprise of the single cylinders seeks and 203 cylinder seeks gain adjustments.

m. Change exerciser program to perform repetitive 203 cylinder seeks and observe gated attention (see Figure 5-55).

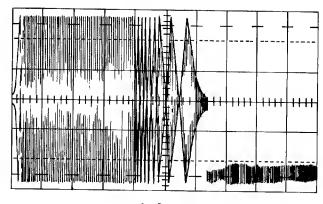PROG: Repetitive 203 Cylinder Seeks
SYNC: Ext   Pos   10 ms   09A05   SKFWD
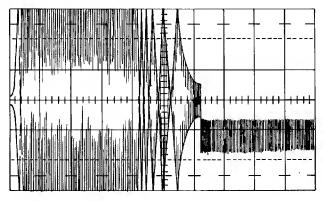CHAN: 1   DC   100 mv 05C04   CYLXDUCER
CHAN: 2   DC   2 v   02B26   GTDATN
MODE: Added
NOTE: The output must be less than 130 millivolts at gated attention time.
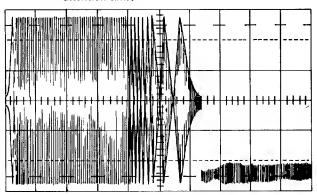

A. Correct

Section 5
Checks, Adjustments and Replacements

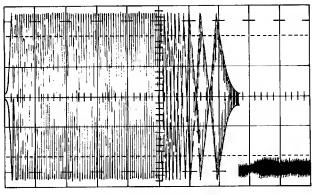B. Incorrect

Figure 5-55. Final Gain Adjustments

n. Readjust POSITION GAIN potentiometer, as required.

o. Maintaining same scope settings, observe and adjust for correct velocity (see Figure 5-56).

PROG:	Repetitive 203 Cylinder Seeks				
SYNC:	Ext	Pos	10 ms	09A05	SKFWD
CHAN:	1	DC	200 mv	05C04	CYLXDUCER
CHAN:	2	DC	5 v	02B26	GTDATN
MODE:	Added				
NOTE:	Velocity must be 65 (−5 +0) milliseconds to gated attention time.				

A. Correct .

B. Incorrect

Figure 5-56. Velocity Adjustment

p. Adjust VELOCITY potentiometer on servo preamplifier, location 13A, bottom potentiometer.

q. Change triggering slope from POS to NEG and readjust VELOCITY potentiometer as required. This ensures that velocity is 65 milliseconds or less, in both forward and reverse directions.

r. Observe and ensure that output of cylinder transducer during repetitive 203 cylinder seeks is within specifications given in Table 5-6, and appears as shown in Figure 5-57.

Table 5-6. Cylinder Transducer Output Specifications

Item	Specification
Average Amplitude (peak-to-peak)	600-1200 millivolts (800 millivolts is ideal).
End-to-End Variation	300 millivolts (600-900 or 700-1000 millivolts).
Tooth-to-Tooth Relationship	20% peak-to-peak of adjacent teeth.
Null during detent	Less than 130 millivolts.
Velocity	60 to 65 milliseconds.

PROG:	Repetitive 203 Cylinder Seeks				
SYNC:	Ext	Pos	10 μs	09A05	SKFWD
CHAN:	1	DC	100 mv	05C04	CYLXDUCER
CHAN:	2	DC	2 v	02B26	GTDATN
MODE:	Added				
NOTE:	Trigger POS for forward and NEG for reverse.				

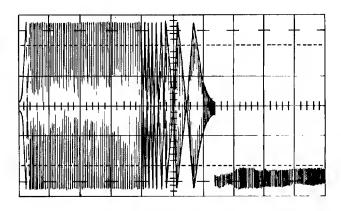**Figure 5-57. Cylinder Transducer Final Check**

s. Power-down disk drive.

t. Remove ac power and remove exerciser.

u. Return disk drive to normal mode of operation.

5-25

DRIVE STATUS MICROSWITCHES

HEADS-EXTENDED MICROSWITCHES

The two heads-extended microswitches provide the controller with the extended or retracted status of the read/write heads and condition the seek logic during a first-seek operation.

Materials required to adjust and/or replace the microswitches are:

- Screwdriver
- Needlenose pliers

Heads-Extended Microswitches Check

a. Turn ac power off.

b. Check that head carriage is in fully retracted position against motor block and disconnect linear motor lead.

c. Extend head carriage forward very slowly until both microswitches "click" simultaneously. Observe that carriage roller has moved forward approximately ¼-inch (see Figure 5-58).
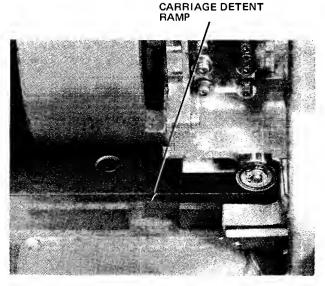

CARRIAGE DETENT RAMP

Figure 5-58. Carriage Detent Ramp

d. Retract head carriage slowly until both microswitches again "click" simultaneously. Observe that carriage is approximately 3/8-inch from fully retracted position.

Heads-Extended Microswitches Adjustment

a. Loosen two screws holding microswitch mounting plate to deck assembly.

b. Move head carriage to a position approximately 3/16-inch from fully retracted position.

c. Adjust microswitch mounting plate until microswitches close. Tighten mounting plate screws and recheck switch closing operation.

d. If not enough adjustment in mounting plate to achieve desired microswitch operation, microswitch lever arms may be formed to achieve desired results (see Figure 5-59).
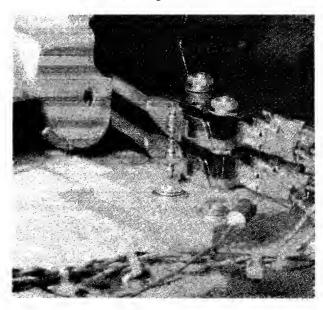

Figure 5-59. Heads-Extended Microswitches

Heads-Extended Microswitches Replacement

a. Label and remove microswitch leads.

b. Remove two nuts attaching microswitches to mounting bracket. Remove microswitches.

c. Stack replacement microswitches on microswitch mounting plate over attaching screw posts.

d. Install and tighten nuts on screw posts.

e. Connect labeled microswitch leads to microswitches. Remove labels.

f. Correct switch wiring may be checked as follows:

Bottom Microswitch (S2)	N.O. — 01B47
	N.C. — 01B23
	Com — Ground
Top Microswitch (S3)	N.O. — 01B41
	N.C. — J13-05
	Com — Ground

RACK-END LIMIT MICROSWITCH

The rack-end limit microswitch is used to monitor the position of the carriage in relation to the end stop. During normal operations, if the carriage is driven to the end stop, the rack-end limit microswitch contacts close causing a seek-unsafe condition.

Materials required to adjust and/or replace the rack-end limit microswitch are:

- Oscilloscope
- Spring Scale (0 — 25 pounds)
- Screwdriver

Rack-End Microswitch Operational Check

a. Monitor output of rack-end limit microswitch and ONRACK flip-flop (see Figure 5-60).

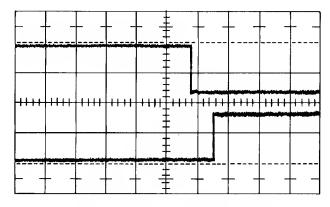| PROG:	Repetitive Restores				
SYNC:	Ext	Pos	1 ms	12A29	VZERO
CHAN:	1	DC	5 v	14A06	LIMITSW
CHAN:	2	DC	5 v	06B11	ONRACK
MODE:	Chopped				
NOTE:	Limit microswitch must fall before **ONRACK** raises.				

Figure 5-60. Rack-End Limit Microswitch Check

b. While performing repetitive restores, ensure that rack-end signal goes low, before ONRACK signal goes high.

Rack-End Microswitch Adjustment

a. Remove air shroud.

·b. Disconnect linear motor lead.

c. Insert lint-free paper between head surfaces.

d. Manually push carriage to end stop.

e. Monitor limit microswitch as follows:

SYNC:	Int	Pos	1 ms	AUTO	
CHAN:	1	DC	1 v	14A02	OFF RACK
CHAN:					
MODE:	CHAN 1 only				

f. Using spring scale, apply pressure to rear of head mounting block (see Figure 5-61).

g. Scope signal must go to ground when pressure is between 20 and 25 pounds.
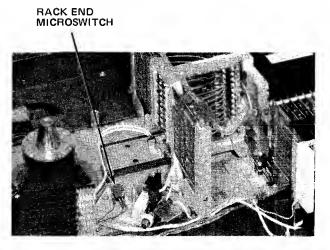
h. Adjust rack-end microswitch accordingly.

RACK END
MICROSWITCH

Figure 5-61. Rack-End Limit Microswitch

Rack-End Microswitch Replacement

a. Remove air shroud.

b. Remove wires from microswitch and label.

c. Remove two screws holding microswitch to sector/index block.

d. To install new rack-end microswitch, reverse procedure.

e. Perform adjustment procedure before reinstalling air shroud.

READ/WRITE SYSTEM

The read/write system (Figure 5-62) has the task of storing data on and retrieving data from the disk pack. When enabled and addressed, the system will accept double-frequency bit serial data and write the data on the disk pack surface in a series of magnetic flux changes. When reading, the magnetic flux changes on the disk pack are sensed and are sent, in double-frequency bit serial format, back to the controller.
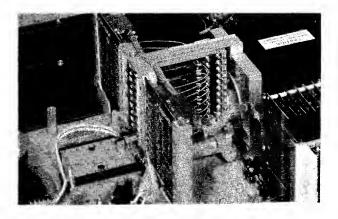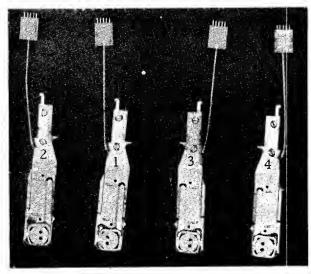

Figure 5-62. Read/Write System

The read/write heads are the means by which data is read from and written onto the magnetic surface of the disk pack. The read/write heads also perform the straddle erase function which maintains the narrow written track width and the maximum track separation essential for optimum playback without crosstalk.

There are twenty heads used in the disk drive with four different configurations of the same basic head assembly. The configuration of each individual head assembly is dependent on whether that head assembly services an upper or lower disk surface, and whether it is mounted on the right- or left-hand side of the head mounting block (see Figure 5-63).

1	91158-001	Head Assy. A Down (1, 5, 9, 13, 17)
2	91158-002	Head Assy. B Up (0, 4, 8, 12, 16)
3	91158-003	Head Assy. A Up (2, 6, 10, 14, 18)
4	91158-004	Head Assy. B Down (3, 7, 11, 15, 19)

Figure 5-63. Four Read/Write Heads

The twenty read/write heads are numbered 00 through 19 and configured as shown in Figure 5-64.

Materials required to perform the following checks on the read/write system are:

● Oscilloscope
● Disk drive exerciser
● Scratch disk pack
● Alignment disk pack

Read/Write System Checks

a. Remove ac power.

b. Install a scratch disk pack and a disk drive exerciser.
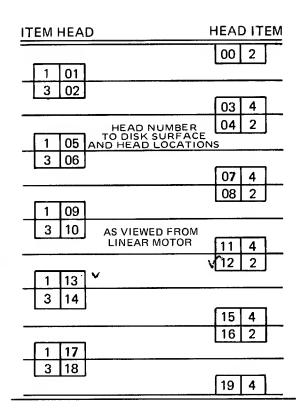
c. Power-up the disk drive.

Figure 5-64. Read/Write Head Configuration

d. Program exerciser to perform a write of "1's" at cylinder 000, all heads (00 – 19).

e. Monitor read data playback.

SYNC:	Int	Pos	1 ms	AUTO	
CHAN:	1	AC	100 mv	02C13	RDDATA
CHAN:	2	AC	100 mv	02C15	RDDATA/
MODE:	CHAN 2 inverted and added				

f. Program exerciser to perform a read at cylinder 000, all heads (00 – 19).

g. Data amplitude must be greater than 150 millivolts.

h. Program exerciser to perform a write of "1's" at cylinder 202, all heads (00 – 19).

i. Program exerciser to perform a read at cylinder 202, all heads (00 - 19).

j. Data amplitude must be greater than 150 millivolts at cylinder 000, and greater than 75 millivolts at cylinder 202. If amplitude is less than specified, read/write head must be replaced. Refer to Read/Write Head Replacement procedure.

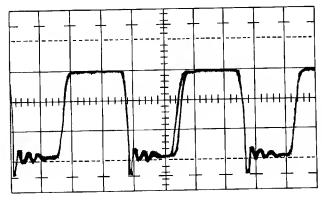k. Monitor output of read data transmitter to check for "jitter" (see Figure 5-65).

PROG: Read Cylinder 202, all heads (00-19)
SYNC: Int   Pos   500 ns   TRIG
CHAN: 1   DC   1 v   02B38   RWDATA
CHAN:
MODE: **CHAN 1** only and multiplied X10
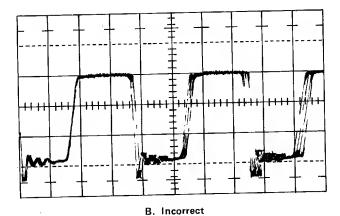NOTE: Jitter must not exceed 50 nanoseconds.

PROG: Read Cylinder 202, all heads (00-19)
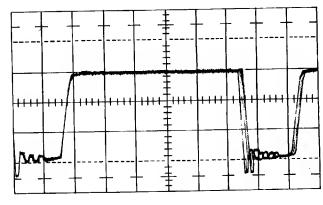SYNC: Int   Pos   500 ns   TRIG
CHAN: 1   DC   1 v   02B38   RWDATA
CHAN:
MODE: **CHAN 1** only and multiplied X10
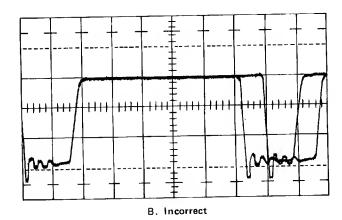NOTE: Jitter must not exceed 50 nanoseconds.

A. Correct

A. Correct

B. Incorrect

B. Incorrect

Figure 5-65. "1's" Jitter Check

Figure 5-66. "0's" Jitter Check

l. If "jitter" exceeds 50 nanoseconds, perform read/write head replacement procedure.

m. Program exerciser to perform a write of "0's" on cylinder 202, all heads (00 – 19).

n. Program exerciser to perform a read on cylinder 202, all heads (00 – 19).

o. Monitor the read data transmitter (see Figure 5-66).

p. If "jitter" exceeds 50 nanoseconds, perform read/write head replacement procedure.

q. Power-down disk drive and remove ac power.

r. Replace scratch disk pack with a CE alignment disk pack.

s. Remove write driver from location 03C and power-up disk drive.

t. Program exerciser to perform a read at Cylinder 73, all heads (00 – 19).

u. Monitor read data playback (see Figure 5-67)

PROG: Read Cylinder 73, all heads (00-19)
SYNC: Ext   Pos   2 ms   03A30   INDEX
CHAN: 1   AC   100 mv 02C13   RDDATA
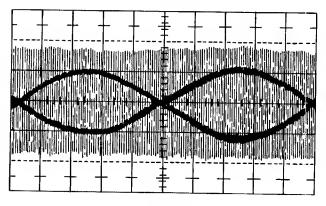CHAN: 2   AC   100 mv 02C15   RDDATA/
MODE: CHAN 2 inverted and added. Sweep-uncalibrated
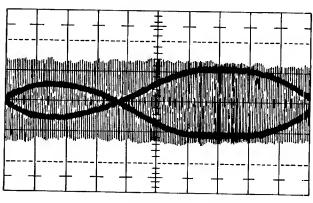   for 25 ms.
NOTE: Crossovers must be at the left, center and right
        vertical graticule and lobe amplitude must be
        within 20 percent of each other.

A. Correct

B. Incorrect

Figure 5-67. Read/Write Head Alignment Check

v. If waveform is incorrect, perform read/write head
    adjustment procedure.

w. Program exerciser to perform a read on cylinder
    118, head 09 or 10.

x. Monitor read data playback (see Figure 5-68).

PROG: Read Cylinder 118, head 09 or 10
SYNC: Ext   Pos   1 μs   03A30   INDEX
CHAN: 1   AC   100 mv 02C13   RDDATA
CHAN: 2   AC   100 mv 02C15   RDDATA/
MODE: CHAN 2 inverted and added. Sweep calibrated.
NOTE: Single "spike" (neg or pos) must be 3 ±2 micro-
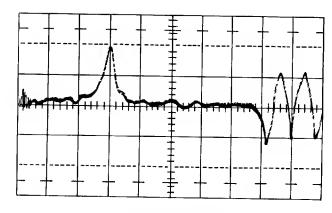   seconds from index on both head 09 and 10.

Figure 5-68. Radial Check

y. If single pulse (positive or negative) is not 3 ±2
    microseconds from index, perform radial
    adjustment procedure.

NOTE

The subsequent check can only be
performed with an alignment disk
pack that has gap scatter data
recorded on cylinder 03.

z. Program exerciser to perform a read at cylinder
    03, all heads (00 — 19).

aa. Monitor read data playback (see Figure 5-69).

PROG: Read Cylinder 03, all heads (00-19)
SYNC: Ext   Pos   2 μs   03A30   INDEX
CHAN: 1   AC   100 mv 02C13   RDDATA
CHAN: 2   AC   100 mv 02C15   RDDATA/
MODE: CHAN 2 inverted and added.
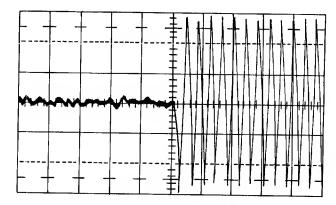NOTE: Data begins 10 ±4 microseconds from Index.

Figure 5-69. Gap Scatter Check

ab. All heads must be 10 ±4 microseconds from Index.
    If a head does not meet this specification, perform
    read/write head replacement procedure.

ac. Power down disk drive and remove ac power.

ad. Remove alignment disk pack and insert write driver in location 03C.

ae. Return disk drive to normal mode of operation.

READ/WRITE ALIGNMENT INFORMATION

Each read/write head on the disk drive has to be aligned so that it is positioned precisely at cylinder 73 on the disk pack. This assures that all read/write heads are positioned to read any disk pack recorded elsewhere, provided the same recording format was used.

Alignment should not be attempted unless the temperature of the disk drive and alignment disk pack is stabilized.

Indicated below are the representative waveforms versus the actual head position in reference to cylinder 73 (see Figure 5-70).

Letters A through E indicate displays of the read envelope under varying conditions of head tracking between cylinders 72 and 74. Compare the relative amplitude of lobes A and B. Correct alignment is shown in letter C. Displays A, B and D, E show these approximate proportions, as shown in Table 5-7.

Table 5-7. Read/Write Head Misalignment

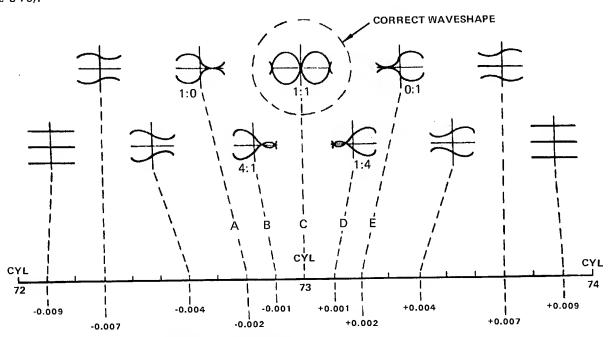| Display	Ratio	Misalignment from Cyl 73
A	1:0	−0.002 inch
B	4:1	−0.001 inch
C	1:1	±0 inch · cylinder 73
D	1:4	+0.001 inch
E	0:1	+0.002 inch

Figure 5-70. Carriage Position Showing 0.001-Inch Increments

Materials required to perform the following checks, adjustments, and/or replacement are:

- Oscilloscope
- Disk drive exerciser
- Scratch disk pack
- Alignment disk pack
- Torque wrench (5.5-inch/pounds)
- Nonmagnetic screwdriver
- Head camming tool

Read/Write Head Tracking Adjustment

a. Remove ac power.

b. Install an alignment disk pack and a disk drive exerciser.

c. Remove write driver from location 03C.

d. Power-up disk drive.

e. Program exerciser to perform a READ on head 00 at cylinder 73.

f. Monitor read data playback (see Figure 5-71).

PROG: Read cylinder 73, head 00
SYNC: Ext   Pos   2 ms   03A30   INDEX
CHAN: 1   AC   100 mv   02C13   RDDATA
CHAN: 2   AC   100 mv   02C15   RDDATA/
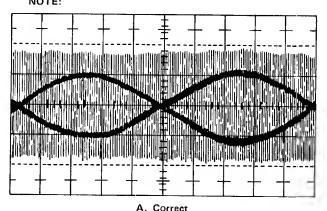MODE: CHAN 2 inverted and added; sweep-uncalibrated
NOTE:

A. Correct

B. Incorrect

Figure 5-71. Read/Write Head Alignment

g. With oscilloscope in uncalibrated position, adjust sweep to display two complete lobes.

h. To adjust head 00, loosen two screws above and two screws below head assembly.

i. Insert a nonmagnetic screwdriver into pryslot at rear of head assembly. Move head assembly in or out until the center crossover is on the center grid when the outer crossovers are on the center grid when the outer crossovers are on the outer grids (Figure 5-71A).

j. Amplitude of the two lobes must be within 20% of each other.

k. Tighten two screws above and two screws below head assembly, with torque wrench (5.5-inch/pounds).

l. Repeat this adjustment procedure for each head by programming exerciser to perform reads on subsequent heads (01 — 19) at cylinder 73.

m. Power-down disk drive and remove ac power.

n. Insert write driver in location 03C and return disk drive to normal mode of operation.

Read/Write Head Radial Adjustment

a. Remove ac power.

b. Install an alignment disk pack and a disk drive exerciser.

c. Remove write driver from location 03C.

d. Power-up disk drive.

e. Program exerciser to perform a read on head 09 or 10 at cylinder 118.

f. Monitor read data/playback (see Figure 5-72).

PROG: Read cylinder 118, head 09 or 10
SYNC: Ext   Pos   1 µs   03A30   INDEX
CHAN: 1   AC   100 mv   02C13   RDDATA
CHAN: 2   AC   100 mv   02C15   RDDATA/
MODE: CHAN 2 inverted and added
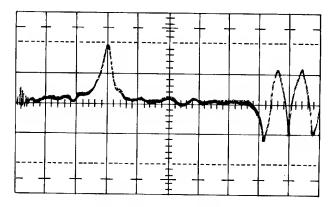NOTE: Single pulse (pos or neg) must be 3 ±2 microseconds from index on both head 09 and 10.

Figure 5-72. Radial Adjustment

g. Adjust radial adjustment nut on sector/index transducer mounting block (see Figure 5-73).

h. Power-down disk drive and simulate opening and closing drawer by moving transducer tilt bar back and forth several times.

i. Power-up disk drive and recheck adjustment.

j. Power-down disk drive and remove ac power.

k. Remove alignment disk pack and insert write driver in location 03C.

l. Return disk drive to normal mode of operation.

CAUTION

Do not allow the sector/index transducer to be torqued away from the disk pack. An emergency retract will result.
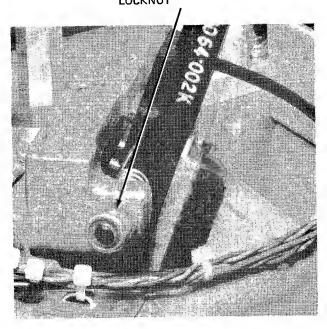
RADIAL ADJUSTMENT
LOCKNUT

Figure 5-73. Radial Adjustment Locknut

Read/Write Head Replacement

a. Power-down disk drive and remove disk pack.

b. Remove ac power.

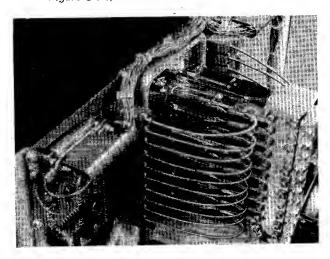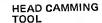c. Remove cable plug of head to be replaced (see Figure 5-74).

Figure 5-74. Read/Write Head Plugs

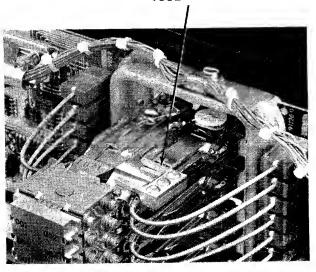d. Install head camming tool on head assembly (see Figure 5-75).

HEAD CAMMING
TOOL

Figure 5-75. Head Camming Tool Installation

e. Loosen two screws above and two screws below the head assembly.

f. Remove read/write head.

g. Install head camming tool on replacement head.

h. Install replacement head fully into head mounting block.

i. Tighten two screws above and two screws below head assembly with torque wrench (5.5-inch/pounds).

j. Perform read/write head tracking adjustment.

k. Perform read/write head gap scatter check.

l. Return the drive to its normal mode of operation.

BRUSH DRIVE

The brush drive assembly (Figure 5-76) is used to clean the disk pack during the power-up sequence. The brush cycle consists of driving the brushes toward the center of the pack, reversing direction, and returning to the retracted position. The drive utilizes the completion of the brush cycle to initiate the power-up initial seek.

Materials required to perform the following checks and/or replacement are:
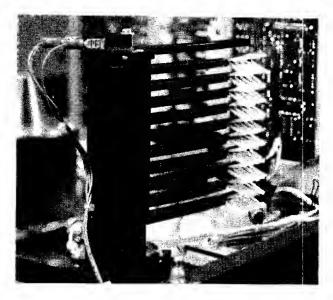
● Screwdrivers

● Needle-nose pliers

Figure 5-76. Brush Drive Assembly

BRUSH DRIVE ASSEMBLY

Brush Drive Assembly Check

a.   Remove ac power.

b.   Install scratch disk pack.

c.   Observe relationship of brush holders to disk pack.

d.   Ensure that brush holders are centered between disk pack surfaces.

e.   Replace brush drive assembly if brush holders are defective.

Brush Drive Assembly Replacement

a.   Remove air shroud.

b.   Remove brush drive motor plug.

c.   Remove two screws holding brush drive assembly to deck plate.

d.   Install replacement brush drive assembly.

e.   Replace brush drive motor plug.

f.   Adjust microswitch to close contact when brush is fully retracted.

g.   Perform brush drive assembly check.

AIR FILTRATION SYSTEM

The air filtration system takes air from the ambient environment, filters and purifies it, and utilizes the purified air to pressurize the disk pack chamber (see Figure 5-77).
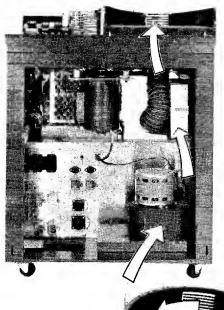

Figure 5-77. Air Flow

The air filtration system comprises the following components (see Figure 5-78):

●   Input Filter

●   Blower Motor Assembly

●   Absolute Air Filter and Plenum
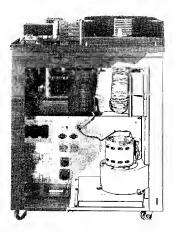
●   Air Shroud and Input Duct

Figure 5-78. Air Filtration System

AIR SHROUD

The air shroud surrounds the disk pack and, with the door closed, forms a positive-pressurized chamber during

operation. The positive pressure in the chamber prevents airborne particles from entering the disk pack area.

Material required to perform the following replacement is:

- Screwdriver (Phillips)

Air Shroud Removal/Replacement

a. Remove four screws that fasten shroud to deck plate standoffs (see Figure 5-79).
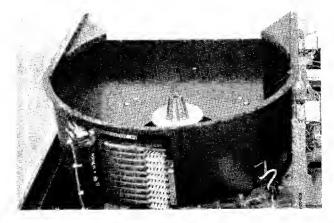

Figure 5-79. Air Shroud

b. Remove shroud by lifting straight up and away.

c. To replace shroud, reverse procedure.

BLOWER MOTOR/AIR FILTER

The blower motor output and the absolute air filter are fastened together by four springs to ensure that a good air seal is formed by their junction.

Materials required to perform the following checks and/or replacement are:

- Air Pressure Gauge
- Screwdriver
- X-acto knife
- Sealing Tape

Blower Motor/Air Filter Check

a. Install disk pack and power-up disk drive.

b. Utilizing pressure gauge, check air pressure at air valve on output plenum (see Figure 5-80).

c. Air pressure gauge must indicate positive pressure. If not, investigate two probable causes:
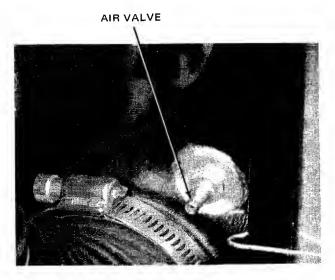
1. Blower Motor

2. Dirty absolute filter

AIR VALVE

Figure 5-80. Air Pressure Check

Blower Motor/Air Filter Replacement

a. Remove blower motor plug P6.

b. Remove four bolts fastening blower motor (see Figure 5-81).
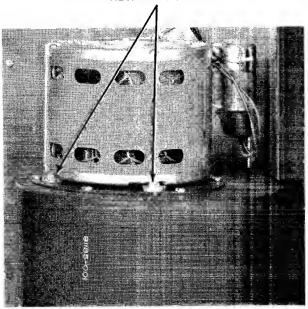
BLOWER MOTOR
RETAINING SCREWS

Figure 5-81. Blower Motor Screws

c. Remove entire assembly.

d. Remove four latching filter springs and disassemble.

e. Replace defective assembly, blower motor or filter.

f. Re-assemble assemblies and install.

g. Replace four holddown screws and connect blower motor plug P6.

CALCOMP

1270 North Kraemer Boulevard, Anaheim, California 92806 714-632-0400